analog dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

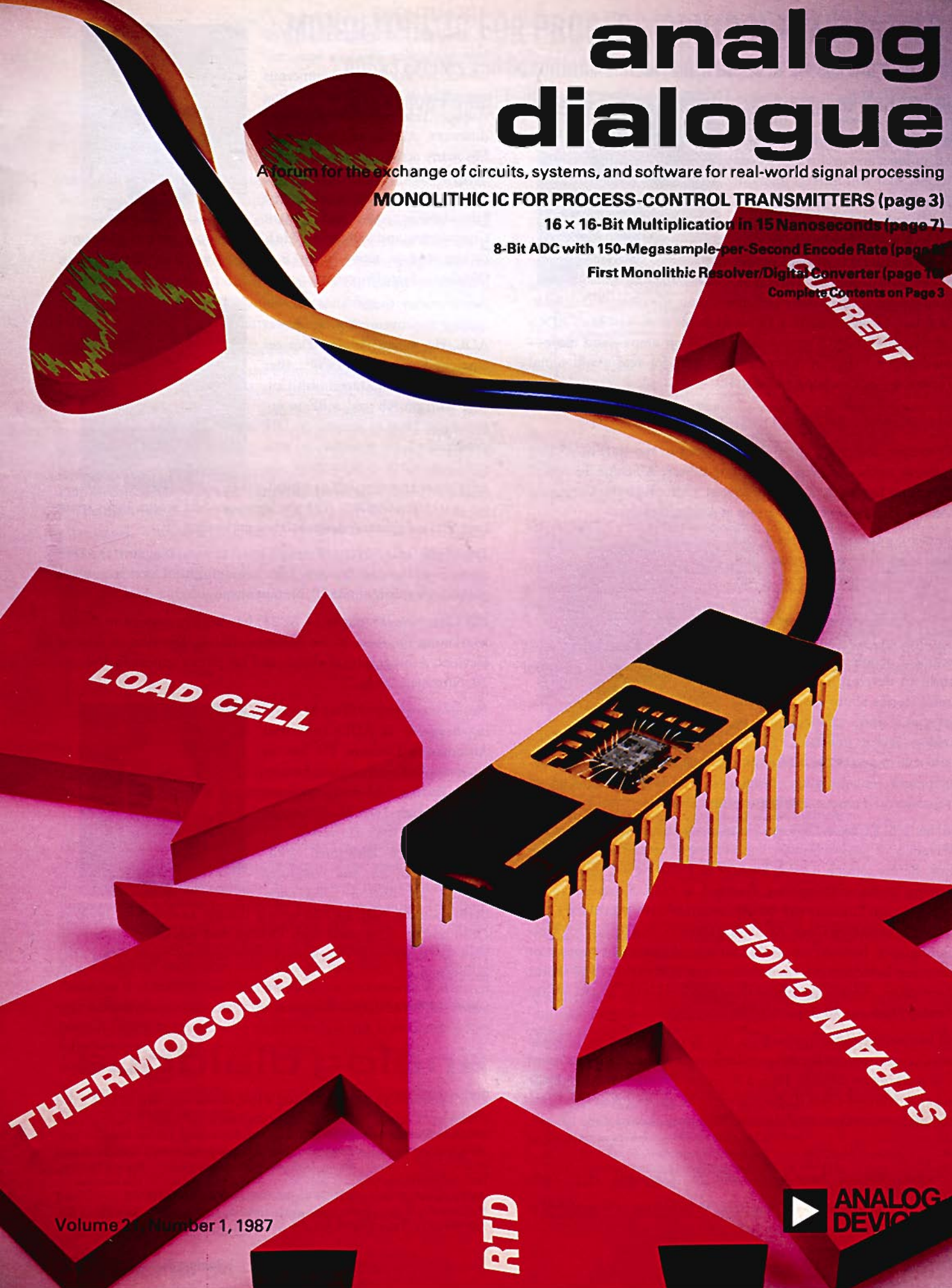
MONOLITHIC IC FOR PROCESS-CONTROL TRANSMITTERS (page 3)

16 × 16-Bit Multiplication in 15 Nanoseconds (page 7)

8-Bit ADC with 150-Megasample-per-Second Encode Rate (page 8)

First Monolithic Resolver/Digital Converter (page 10)

Complete Contents on Page 3



Volume 21, Number 1, 1987

ANALOG DEVICES

Editor's Notes

SPEED

Our cover theme is the AD693 monolithic analog IC for process-control transmitters—an innovative, unique, and useful signal conditioner that will interest many of our readers. But if you think this issue of *Analog Dialogue* is all about dc signal conditioners, take a look at the table of contents on the opposite page. You'll find that, *au contraire*, if there's any common theme for most of this issue, it's *speed*. From 15-ns 16 × 16-bit multipliers to 150-Ms/s ADCs and 300-MHz DACs to 1.4-GHz GBW op amps—and more—you'll find a world of really fast products for real-world signal processing—both analog and digital.

BILL SCHWEBER, CONTRIBUTING EDITOR

We are pleased to welcome Bill Schweber to the staff of *Analog Dialogue* in the role of Contributing Editor. A Senior Technical Marketing Engineer, Bill is the newest addition to the Corporate Technical Communications group at Analog Devices.

Besides contributing counsel and articles to this publication, Bill works with engineers at all levels and locations within Analog Devices, with editors of trade publications, and with a wide range of technical people elsewhere in the world to develop interesting and useful stories about designs, technologies, and applications of Analog Devices products. He also has a role in one of the most important aspects of professional development—encouraging, stimulating, and helping engineers to overcome their reticence to write technical articles.

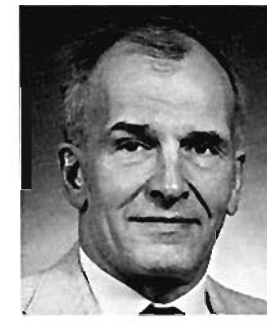
Bill has a BSEE from Columbia University and an MSEE from the University of Massachusetts, specializing in communications systems. Before joining Analog Devices in 1980, he had served as a Systems Engineer (telephone systems) at GTE Sylvania, and a Senior Design Engineer (μP-based materials-testing hardware and software) at Instron Corp. At Analog Devices, as a Senior Marketing Engineer, he was responsible for introduction and support of computer-based systems for measurement & control of real-world phenomena; the most recent of these products is the μMAC-6000 (*Analog Dialogue* 20-2, pp. 10-13).

Bill has written numerous articles that have appeared in the trade press, several articles for this publication, and two textbooks[1] (and he is working on a third). He is a Registered Professional Engineer and an Advanced-Class Radio Amateur; he also holds a First-Class Radiotelephone Operator's license. Welcome aboard, Bill!

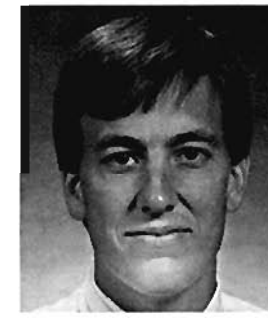
Dan Sheingold

[1]Schweber, William, *Integrated Circuits for Computers*. New York: McGraw-Hill, 1985.
———, *Data Communications*. New York: McGraw-Hill, to be published in 1987.

ADI AUTHORS



A. Paul Brokaw (page 3) is a Fellow at Analog Devices Semiconductor. He has designed numerous successful IC products, including voltage references, signal conditioners, ADCs, and amplifiers. His many activities include circuit design, new-product definition, contributions to the work of the Education-Support and Patent Committees, and mentoring. He has numerous patents and publications and is active in IEEE. He has a BS in Physics from Oklahoma State University.



Jim Doscher (page 3) works on quality improvement programs at ADI. He joined Analog Devices Semiconductor in 1982 after graduating from Dartmouth College with an AB and a BE in engineering. Prior to joining the QIP department, he worked on new products as a product/test development engineer and as a product marketing engineer with the linear product group. In his spare time, Jim is a skiing and windsurfing enthusiast.

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Bill Gotschewski (pages 14 & 23) has been promoted to Senior Marketing Engineer in the Microelectronics Division of Analog Devices. A biographical sketch and his photo appear in Volume 20, Number 1 (page 2).

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(More authors on page 30)

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MONOLITHIC IC FOR PROCESS-CONTROL TRANSMITTERS

AD693 Excites and Conditions Sensor, Interfaces to 20-mA Current Loop Uses Loop Power; Includes Auxiliary Amplifier, Scaling, and References

by A. Paul Brokaw and James Doscher

Although the digital transmission of data is a widely discussed technique in modern data-acquisition systems, many applications convey remote information effectively and economically using *analog* signals. In process control, controlled currents with spans of 4 to 20 mA or 0 to 20 mA carry analog data for long distances over two wires (0-to-20 mA loops need a third lead for power), representing such sensor variables as temperature, pressure, speed, or flow with accuracy, reliability, and low cost.

Such loops are much less susceptible to noise pickup than circuits in which voltage levels carry the information, because they ignore common-mode levels and voltage drops; the high source impedance minimizes the effect of induced voltages; the twisted pair tends to reject common-mode current pickup; and the low loop-termination impedance (typically 250Ω) minimizes the effects of leakage current and capacitively coupled noise. The sensor-to-loop circuitry can be powered from the remotely located loop supply by the 4 mA share of 4-to-20-mA loop current that represents zero signal, without additional power supply or wires, since the wires convey both information and power (Figure 1). Any break in the two-wire loop can be quickly detected in the control room, since the loop current drops to zero from the normal non-zero value.

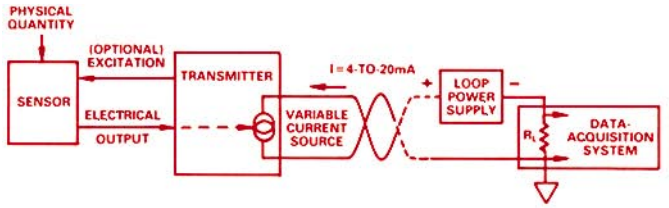


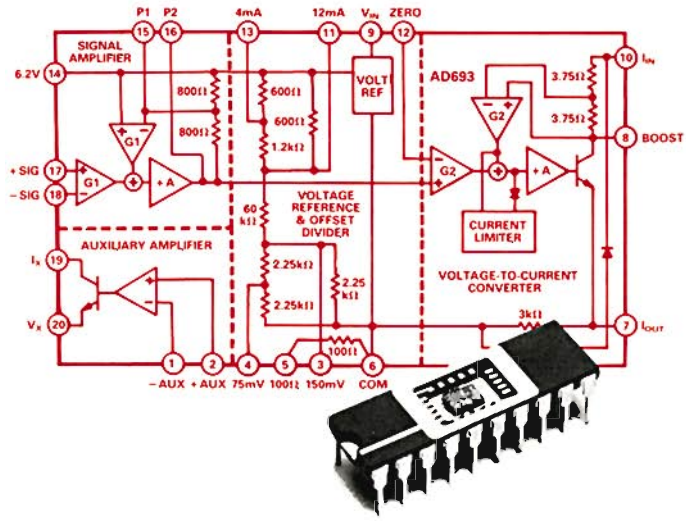
Figure 1. Basic current-loop configuration for sensor, transmitter, loop wire, loop power supply.

TRANSMITTER PROBLEM AND SOLUTION

Design of the transmitter, which interfaces between the sensor and the loop, faces demanding requirements. If the sensor is a passive device, such as a strain gage or RTD, it may need excitation; its output signal must be amplified by a differential-input amplifier, since the output is usually small and generally floats at a common-mode voltage level. Sensors having differing electrical characteristics, ranges of excitation, and scale factors must be accommodated, so that the buffered and amplified signal may be converted into a controllable current at the standard output level. The entire interface must consume little power; only 4 mA is available when loop-powered, and much of that current may be needed for exciting the sensor.

Transmitters are available commercially in modular form, often with high-voltage isolation (e.g., the Analog Devices 5B39 and devices in the 2B and 3B series). In another popular approach, they are designed by the user in pursuit of illusory cost savings; the result quite frequently tends to be relatively large, expensive, and complex: portions of circuit boards harboring discrete ICs, transistors, passive components, and adjustment "tweaks."

*Use the reply card for technical data.



The AD693,* a complete monolithic solution in a 20-pin DIP, provides compact and low-cost excitation, conditioning, ranging, and transmission. It includes pin-strapped ranges and features that minimize the number of external components required. When powered from the 4-to-20-mA loop current, it can provide up to 3.5 mA of sensor excitation. The loop power supply can range from 12 to 36 volts. A local supply, separate from the two-wire loop, can also be used (sometimes called "three-wire operation").

IN THIS ISSUE

Volume 21, Number 1, 1987 – 32 Pages

Editor's Notes, Authors . . . 2
Monolithic IC for Process-Control Transmitters (AD693) . . . 3
16 × 16-Bit Multiplication in 15 Nanoseconds (ADSP-8018/7018) . . . 7
8-Bit ADC with 150-Megasample-per-Second Encode Rate (AD9002) . . . 8
8-Bit, 300-MHz Monolithic D/A Converter for Displays (AD9703) . . . 9
First Monolithic Resolver-Digital Converter Provides 12-Bit Outputs (2S81) . . . 10
Monolithic Precision Voltage Reference (AD588) . . . 12
Quad 12-Bit Readback DAC with 40-ns Bus-Access Time (AD392) . . . 14
New DSP ICs for Increased Functionality and Performance . . . 15
High-Speed Integer Arithmetic Chip Combines Numeric Operations (ADSP-1101) . 16
Multiport Register File Speeds DSP Systems, Reduces Chip Count (ADSP-3128) . 17
High-Speed Floating-Point Multipliers and ALUs Follow IEEE-754 . . . 18
High-Speed 24 × 24 Multiplier Performs Computation in 95 ns (ADSP-1024A) . . 20
Single-Port Multiplier/Accumulator in a 28-Pin Low-Cost Plastic DIP . . . 21
Wide-Bandwidth, Fast-Settling Operational Transimpedance Amplifier (AD9610) . . 22
High-Speed Pin Driver for Digital Device Testing (AD345) . . . 23
Modular I/O Card for the IBM PC (RTI-820) . . . 24
Process Monitoring & Operator Interface Software for μMACs (CAMM) . . . 25
Precision Signal Conditioner for Bridge Transducers (1B32) . . . 27
New-Product Briefs:
CMOS Switches–4 Quad SPST Devices (ADG201A/202A, ADG221/222) . . . 28
Monolithic Op Amp Settles to 1% in 12 ns (AD5539) . . . 28
CMOS Dual 8-Bit Multiplying DAC, TTL/CMOS-Compatible (AD7628) . . . 28
New Software Release for RTI-800 Series (AC1527-A) . . . 29
ASYST for RTI-800–Application Software: Lab, Scientific Data Acquisition . . . 29
Test Development Station for Benchtop Testers (LTS-2020TDS) . . . 29
New Literature, More Authors . . . 30
Potpourri . . . 31
Advertisement . . . 32

The instrumentation-amplifier front end is pre-calibrated for 30- and 60-mV input spans, ±15 and ±30-mV input spans, and for 100-ohm platinum RTDs. The part may be trimmed to other spans, ranging from 1 mV to 100 mV, to handle most sensors. Pre-calibrated output spans include 4-20 mA, 0-20 mA (local, not loop power), and 12 mA ± 8mA.

In addition, the circuit configuration of the AD693 permits cold-junction compensation (CJC) for thermocouples, as well as simple, first-order linearization for many types of sensors. The current loop can be driven directly, or through an external pass transistor connected to the AD693's Boost (Figure 2). This feature reduces on-chip power dissipation, resulting in extended operating temperature range, enhanced reliability, and minimal self-heating errors. The external pass transistor diverts most of the loop current around the IC, allowing loop currents of up to 50 mA.

STRUCTURE OF THE AD693

In Figure 2, the AD693 is shown connected for a 0-30mV unipolar input and 4-20mA output. It has three major functional blocks: An *instrumentation-amplifier* front end buffers and scales the low-level input signal. This signal amplifier is connected to a *voltage-to-current (V/I) converter*, which drives the current-loop output. A precision 6.2-volt *reference and resistive divider* provides voltages for setting the selectable zero point and span of the output scale and serves as an excitation source for sensors.

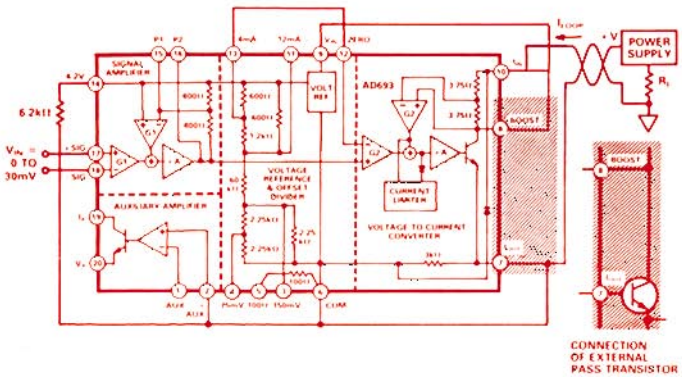


Figure 2. Block diagram of AD693, with minimal connections for 0-30mV input and 4-20mA output. The inset shows how an external pass transistor can be used to off-load most of the dissipation.

The signal amplifier has two differential-input amplifiers, which sum into a high-gain output stage. The input signal is differenced with a fed-back version of the output; the net result drives the high-gain amplifier, which tends to keep its input at zero; for this to happen (with equal gains), its output must be equal to the differential input signal. The V-to-I converter uses a similar pair of amplifiers and works in the same way, except that the output from the input-signal amplifier is offset and compared with the voltage developed across a resistor in series with the output current; the comparison drives the current so as to set the net difference equal to zero, hence the current is offset and proportional to the input voltage.[1]

A 0-to-75-mV signal applied from the signal amplifier results in a 0-to-20-mA loop current. Normally, 15 mV is applied internally to offset the zero point at 20% of the range, i.e., 4mA; this lets a 0-to-60mV range correspond to a 4-20-mA span. A 30-mV span can be handled by changing the jumpering pins of the IC for a different scale factor. Other pin-strap options provide 0 mA or 12 mA of offset current for the loop.

The AD693 also has an auxiliary amplifier; it can be used to attenuate or amplify the reference voltage and provide constant-current excitation or match the sensor-excitation voltage to the sensor's specific requirements.

When an external pass transistor is used (Figure 2), it diverts the loop current around the AD693 to reduce self-heating and improve device performance over the industrial temperature range. Loop current from I_{OUT} drives the base of the transistor, which should have BV_{CEO} greater than the supply voltage and a power rating sufficient to handle 25 mA at the supply voltage. Types 2N1711, 2N2219A, and 2N3440 are good candidates.

THERMOCOUPLE INTERFACE WITH THE AD693

The thermocouple is the most common sensor for measuring temperature over wide ranges. Two dissimilar metals produce a small but repeatable voltage as a function of temperature.[2] For example, a type-J thermocouple uses iron and Constantan wires; its sensitivity is about 50μV/°C. When a thermocouple is used as an input to a data-acquisition system, the resulting signal is in the millivolt range and is often accompanied by noise.

Besides amplification, thermocouple outputs often require "cold junction compensation (CJC)." The connection point of the thermocouple leads and their termination points (usually plated screws) creates another set of miniature thermocouples at the termination panel's ambient temperature (usually a much narrower range of temperatures than those being measured, typically in the vicinity of "room" temperature). The voltage generated at this "cold" junction must be compensated so that the net voltage used for the actual temperature reading is only that of the thermocouple junction itself. Many of the various techniques used for CJC are compatible with the AD693.

Figure 3 shows a thermocouple interface and typical cold-junction compensation using the AD693; an AD592 low-cost, precision semiconductor-based temperature transducer senses the temperature near the thermocouple termination points and produces a current output of 1μA/K. Type-J thermocouple sensitivity at room temperature is 52μV/°C, so a 52-ohm resistor is used to convert the AD592 output to a 52-μV/°C temperature-dependent CJC voltage. The CJC voltage is subtracted from the thermocouple output to cancel the voltage generated by ambient temperature at the

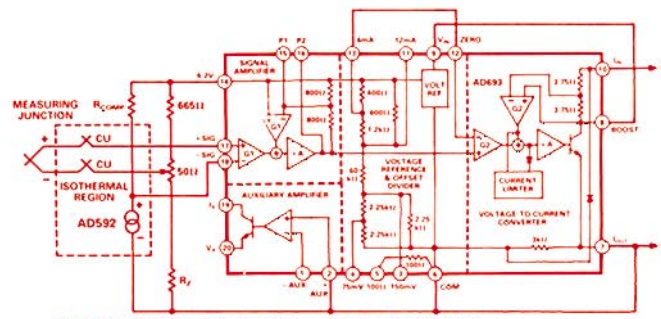


Figure 3. Thermocouple input; the AD592 temperature sensor is used for cold-junction compensation.

[1]See *Electronic Design*, April 18, 1985: "Versatile Transmitter Chip Links Strain Gages and RTDs to Current Loop," by Paul Brokaw, for greater detail.

[2]For information on popular transducers and techniques for interfacing them to data-acquisition systems, see ADI's *Transducer Interfacing Handbook* (1980).

termination screws; thus the input amplifier sees only the voltage variation due to the thermocouple temperature. The 50-ohm potentiometer circuit provides the correct zero-adjustment range and translates the Kelvin scale of the AD592 to degrees Celsius. Calibration is done by putting the thermocouple in an ice bath (0°C), or using a thermocouple simulator, and adjusting for loop current of 4 mA. A thermistor or diode can also be used as the ambient temperature sensor for CJC.

This circuit provides an upscale indication of any break or open circuit in the thermocouple or leads. If the wire is broken, the bias current flowing out of pin + SIG attempts to flow through the infinite impedance at the break, substantially increasing the voltage at + SIG relative to that of − SIG, and output current is >20mA. Downscale break-detect can be achieved with a different connection configuration.

CONNECTION WITH RTDs

The RTD (*resistance temperature-detector*) is often used for temperature measurement because of its high accuracy and repeatability. A standard platinum RTD has a resistance of 100 ohms at 0°C and a temperature coefficient, $\alpha = 0.00385$. The AD693 can interface directly to RTDs, as shown in Figure 4. The 3-wire RTD and the temperature-stable 100-ohm resistor built into the AD693 form a feedback network around the auxiliary amplifier; the closed-loop non-inverting gain is $(1 + R_T/100\ \Omega)$, where R_T is the resistance of the RTD. The "+" input of the auxiliary amplifier is connected to the 75-mV tap of the voltage divider.

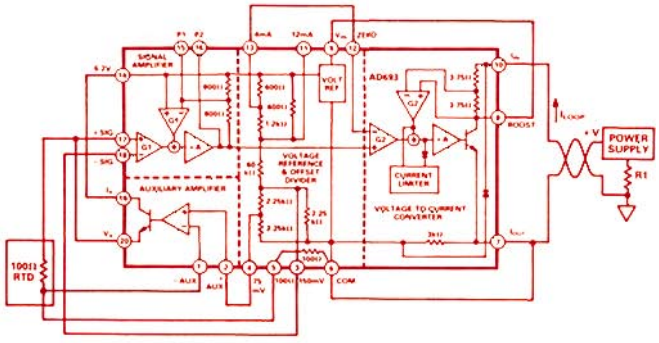


Figure 4. AD693 configured as 0°-to-104°C RTD interface with 4-20mA output.

At 0°C, the 100-ohm RTD resistance results in an amplifier gain of +2, so V_X is 150 mV. The input signal amplifier compares this to the 150-mV divider tap, and a zero differential signal results. As the temperature (and resistance of the RTD) increases, the output of the auxiliary amplifier will increase due to the increase in gain, which changes in proportion to the RTD resistance. The difference between this voltage and 150 mV drives the amplifier to modulate the loop current. The AD693 is pre-calibrated to provide 4 to 20 mA over a 0°C to 104°C range, in response to an RTD resistance increase to 140 ohms, and a resulting differential input voltage of 30 mV. There are five other pre-calibrated pin-strap range options, from (−100.6° to 103.9°) to (+51.6° to +266.4°).

STRAIN GAGES AND LOAD CELLS

A resistance strain-gage has resistance that varies with the strain that results from applied stress or load. It is used, generally in a bridge circuit, for measuring force, pressure, or displacement. The AD693 can provide the required excitation and amplify the floating voltage that results. When the applied load is unidirectional, the loop current range represents 100% of span; for bidirectional loads, the loop is often set up so that 12 mA represents no load, 4 mA is −100%, and 20 mA equals +100% of span.

A typical strain gage produces a full-scale output-voltage change of 2 mV per volt of bridge excitation. The 6.2-volt reference of the AD693 can be used to power the bridge directly when the bridge impedance is high enough that the maximum current capability of the reference is not exceeded (typically, 3.5 mA for loop-powered operation and 5 mA when remote power is supplied)*. The relatively low output voltage from the bridge, about 12 mV, requires that the span of the AD693 input amplifier be reduced to match the 20-mA loop output to the full-scale bridge output. Also, it is desirable to calibrate the AD693 input to the output of the specific strain-gage element used. Here are techniques for doing this:

Span Adjustments

The input amplifier amplifies or attenuates the sensor signal so that the V-to-I section receives a 60-mV signal, which is then converted to a 16-mA output signal (plus 4-mA offset) for the current loop. With P1 & P2 shorted, the signal amplifier's gain is unity; this condition is met for 60-mV input. With pins P1 & P2 open, the gain is increased to 2, and 30-mV in produces a 60-mV output.

To accommodate other gain ranges, or adjust for variations in individual sensor outputs, the voltage divider at the output of the signal amplifier between pins P2 and 6.2 V can be adjusted. For spans of less than 30 mV, an external resistor, RS1, is used in parallel with R_a (Figure 5) to increase the closed-loop gain of the signal amplifier, so that a smaller sensor voltage will correspond to the full-scale span of the V/I converter. The value of the external resistance, R_{S1}, between P1 and the 6.2-V point, should be:

$$R_{S1} = \frac{400\ \text{ohms}}{\frac{30\ \text{mV}}{S} - 1}$$

where S is the desired span. For a span of 12 millivolts, S = 12 mV, and $R_{S1} + 400/(2.5 - 1) = 267$ ohms.

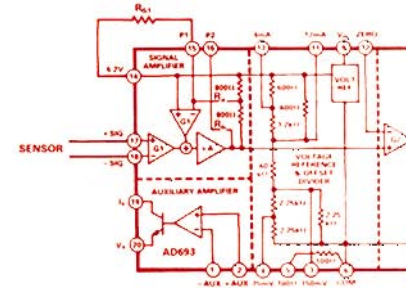


Figure 5. A resistor, R_{S1}, connected between P1 and 6.2V, increases the gain of the signal amplifier. A resistor connected between P1 & P2 decreases the gain of the signal amplifier to accept larger signals than the preset span allows.

For ranges between 30 mV and 60 mV, a resistor is placed in parallel with R_b (i.e., between pins P1 and P2) to reduce the gain of the signal amplifier. A different formula is used to calculate this resistance (see the data sheet for details).

Some caution must be used, since the temperature coefficient of the external trim resistors may differ from the relatively low −17 ppm/°C coefficient of the resistors inside the AD693. Also,

*For lower-impedance bridges, such as the common 350-ohm type, the reference voltage can be reduced through a voltage divider and the auxiliary amplifier used to provide a stiff drive.

the internal resistors are trimmed for high resistance-ratio accuracy, but the absolute resistance may vary from nominal by ±10%. An extra 10% trim range and potentiometer adjustment will usually be required, and the external scaling resistance value should be picked to permit the addition of a series trim.

Offset Adjustments

The offset adjustments for the output range are selected by connecting the appropriate tap of the divider network of the 6.2-V precision reference to the inverting input (pin 12) of the V/I converter. The AD693 provides pre-calibrated voltages corresponding to zero offsets of 0 mA, 4 mA, and 12 mA, using pins 14, 13, and 11. The various combinations of AD693 pin-strapping options result in six combinations of input and output span. Other offsets can be obtained, or the offset can be made adjustable (for sensors whose zero output does not correspond with the desired span zero point), by means of a separately wired voltage divider, driven from the 6.2-V reference.

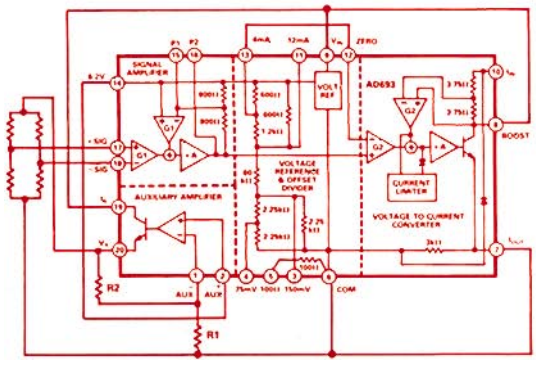


Figure 6. Resistors R1 and R2 on the auxiliary amplifier are used to change the gain of the amplifier when, for example, the excitation value for the sensor must be scaled.

Using the Auxiliary Amplifier

The versatile auxiliary amplifier provides another possible approach to span adjustment. If the sensor requires excitation from the AD693, the auxiliary amplifier can be used to provide an adjustable excitation value, which can be trimmed so that the resulting sensor output matches one of the inherent ranges of the signal amplifier. Suppose the sensor is a high-impedance strain gage with 4 mV/V sensitivity. Its full-scale output, using the 6.2-V reference, will be 24.8 mV. The auxiliary amplifier can be configured with a noninverting gain of 30/24.8 = 1.21, to amplify the reference to $6.2 \times 1.21 = 7.5$ V, with resistors R1 and R2, as shown in Figure 6. Pins P1 and P2 are left open to select the 30-mV span of the signal amplifier. For sensor outputs that differ from the nominal value, the auxiliary amplifier's feedback resistance should be less than nominal and a trim potentiometer used in series for final adjustment.

The auxiliary amplifier can also be used as a current source for sensors that require current excitation for best performance. A monolithic pressure sensor, such as the Model 23 from IC Sensors (Sunnyvale, CA), includes an internal calibration resistor that makes individual units interchangeable. This resistor is used with the AD693's auxiliary amplifier to make a bias network to insure that the full-scale output of the sensor is 60 mV (Figure 7). Current is determined by the voltage, V_X, across the AD693's 100-ohm resistor, with the auxiliary amplifier configured as a current source. The voltage is equal to the output of the voltage divider, consisting of the sensor calibration resistor, R_{CAL}, and an external, user-supplied 101-ohm resistor, R2. The sensor output then needs no span adjustment. Any zero-offset in the sensor can be trimmed by setting the output to 4 mA with R_Z.

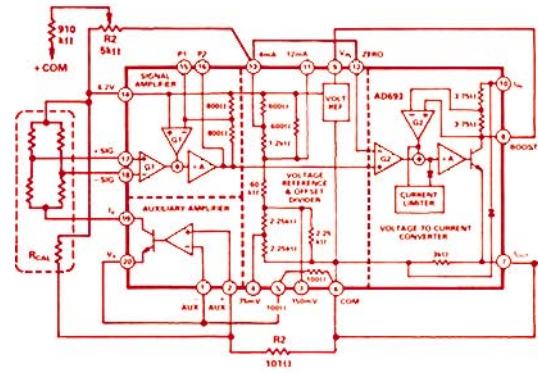


Figure 7. The auxiliary amplifier can be used as a current source that also normalizes the full-scale output of the sensor, using the sensor's internal calibration resistor.

Linearization

Many transducers provide an output signal that is not linear with changes in the input variable being sensed, because of either an inherent characteristic of the transducer or imperfections in the practical sensor realization. The AD693 can often be configured to compensate for some types of nonlinearity, at least partially, over the range of interest or greatest deviation, by making use of the modulating (i.e., multiplication) effect of the excitation voltage. Part of the sensor output can be fed back to provide a parabolic correction, using the auxiliary amplifier to sum the correction voltage and the sensor excitation signal (see Figure 5.9a in the *Transducer Interfacing Handbook*).

Local Power

Although the AD693 can be powered from the 20-mA signal loop, there are applications where it is preferable or necessary to use a local power supply, connected as shown in Figure 8. The 0-20mA range offers two potential advantages: simplification of the loop receiver and a 25% increase of effective resolution. A local supply must be used for 0-to-20-mA loop output, since at 0 mA there is no power available for internal use and transducer excitation. In the 0-to-20-mA configuration, the precalibrated input spans change from 30 mV to 37.5 mV, and from 60 mV to 75 mV.

The external pass transistor (Figure 2 inset) permit loop currents greater than the 20-mA maximum. In the local supply connection, with a 5-ohm resistor across I_{IN} and Boost pins, the loop-current sampling ratio within the AD693 is changed. The V-to-I converter sees a different range factor as it meters the loop. The loop current can then increase by a factor of 2.5, from 0 to 50 mA or 10 to 50 mA.

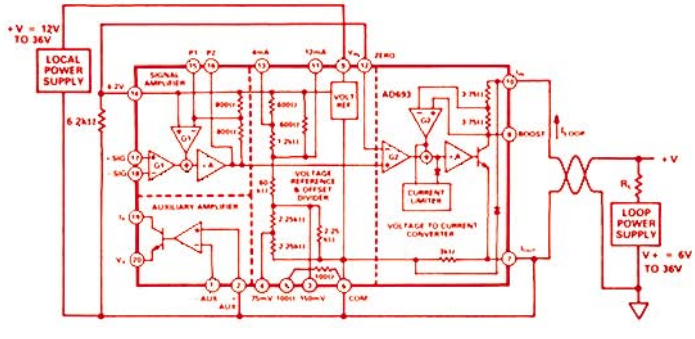


Figure 8. Connection to operate with local power.

16 × 16-BIT MULTIPLICATION IN 15 NANOSECONDS

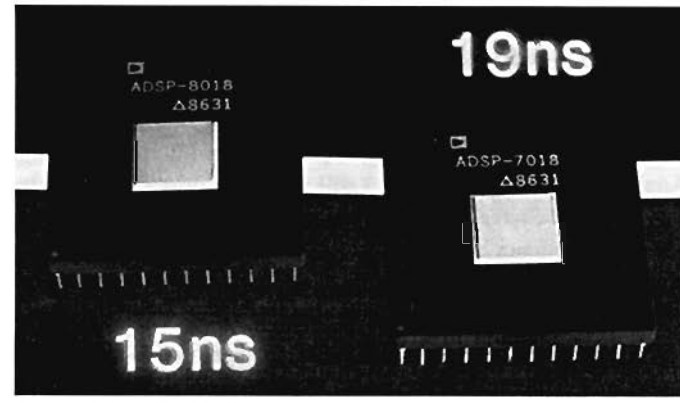
ECL-Compatible (15 ns) ADSP-8018 and TTL-Compatible (19 ns) ADSP-7018 Employ Innovative Architectural Features in Bipolar Technology

by David Fair

The ADSP-7018 and ADSP-8018* are 16 × 16-bit multipliers designed for ultra-high-speed digital signal-processing and number-crunching applications, using one of the fastest bipolar integrated technologies available. They are designed for use in array processors, digital filtering, image processing, and graphics applications, which require extremely short multiplication times and permit fixed-point multiplication. Unique architectural enhancements, discussed below, increase the versatility of these ICs; they use bipolar technology to achieve 19-ns (ADSP-7018) and 15-ns (ADSP-8018) multiplication times. The ADSP-7018 is TTL compatible, while the ADSP-8018 is ECL 10KH compatible.

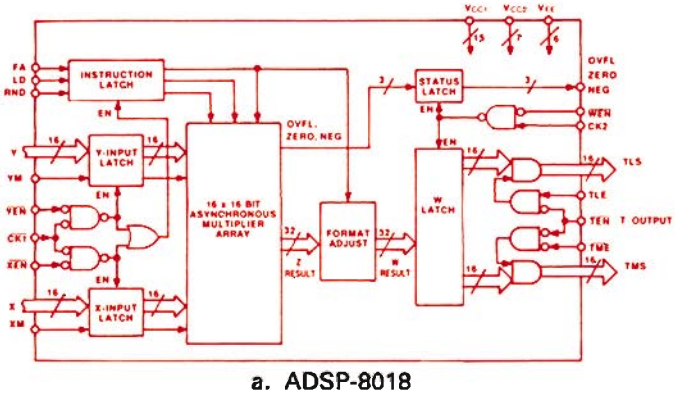
Both multiplier ICs are functionally similar four-port devices with two 16-bit input ports and a 2 × 16-bit output port. The 32-bit products are available in parallel, as independently enabled MSP and LSP fields (-7018 and -8018), or with LSP and MSP multiplexed to a single 16-bit port (-7018 only). Each 16-bit field of the product latch has its own three-state output control. The design of these ICs seeks to take every precaution required for these speeds: there are multiple power and ground paths within the IC, and different sets of external power and ground pins are used for the internal logic and output circuits.

A variety of data latching options can be selected. The input operands and output results are stored in individually enabled latches with separate, independent clocks for input and output. *Asynchronous* (unclocked) flow-through operation can be obtained simply by making the latches transparent, with the clocks and enables held active. The multiplication result appears at the output pins as soon as the multiplication operation has been performed by the internal logic. To simplify *synchronous* operation, both clocks are tied together as a single clock which causes the input and output latches to operate in complementary fashion. With both clocks held to the active state, the three latch-enable controls can function as three independent clock lines for the two data input ports and the output port. Thus, the user can choose among unclocked, single-, double-, and triple-clock operation.

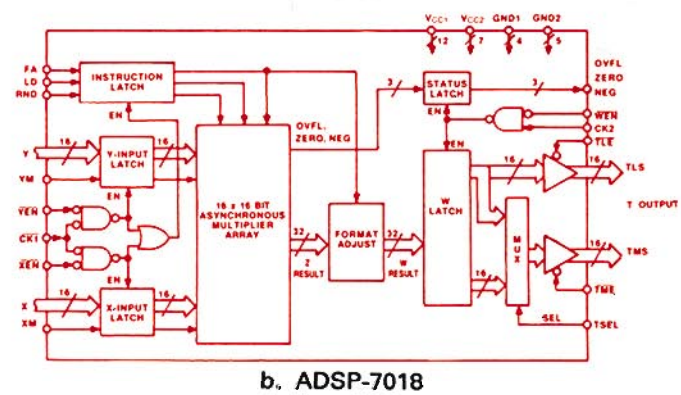


A choice of number formats is also available. The X and Y input data can be either in twos-complement, unsigned-magnitude, or mixed-mode formats. Outputs are in the same format as inputs, unless the input formats are mixed; in that case, the outputs will be in twos-complement representation. The 32-bit product can be format-adjusted for consistent signed fractional output format and for maximum precision in a 16-bit MSP: the MSP of the format-adjusted 32-bit product can be rounded, instead of merely truncated, by a control which causes a 1 to be added to the most-significant bit of the LSP. Three status flags indicate the presence of a zero, negative, or overflowed result. The input operands can be loaded and passed through directly without multiplication, but with format adjustment, rounding, and setting of status flags.

The ADSP-7018 (TTL compatible) also has a multiplexer, which permits the 32-bit result to be written onto a single 16-bit bus in two bytes, if desired. Power consumption is a maximum of 4.0 W, with the nominal +5-V supply. The ADSP-8018 (ECL compatible) requires 4.125 W maximum with a −5.2-V supply. Both devices are housed in a 108-pin grid-array package and specified over the 0 to 70°C commercial temperature range (device suffix JG). An ambient airflow of approximately 500 linear feet per minute (about 2¾ meters per second) is required. Price (100s) is $205 for the ADSP-7018JG, $260 for the ADSP-8018JG.



a. ADSP-8018



b. ADSP-7018

Figure 1. Block diagram of the ADSP-8018 16 × 16 multiplier (a) shows the two 16-bit X and Y input ports and the 32-bit T output, along with control, status, power, and ground lines. The ADSP-7018 (b) differs principally in the output port, which can also present the data as two 16-bit multiplexed products.

*Use the reply card for technical data.

8-BIT ADC WITH 150-MEGASAMPLE-PER-SECOND ENCODE RATE

AD9002 Has Low Input Capacitance, 17 pF; Wide Bandwidth, 115 MHz (−3 dB) Power Requirement is Only 750 mW; Single −5.2-Volt Supply

by Alan Hansford

The AD9002* is an 8-bit, high-speed monolithic flash a/d converter, featuring a top encoding rate of 150 megasamples per second (125 min). Besides its excellent basic speed-resolution specification, its input capacitance is a low 17 pF (22 pF max), making it easy to drive; and, with a single supply of −5.2 volts, it typically dissipates a low 750 milliwatts, simplifying excitation and cooling. Analog signal bandwidth (−3 dB) is a comfortable 115 MHz, which means decreased error for signals at frequencies below the Nyquist frequency (75 MHz when sampling at 150 MHz). The wide analog bandwidth, due to a new comparator design, is a byproduct of the extremely dense bipolar processing technique.

Applications for such fast flash ADCs include the wide range of signal-acquisition uses that require high-speed digitizing of analog and pulse waveforms. Specific applications include digitizing oscilloscopes, spectrum analyzers, communication equipment, and automatic testers. Since speed is an essential requirement in defense systems, there are many applications in radar, guidance, and warning systems.

The AD9002 comprises 256 parallel comparators with outputs decoded to drive the ECL-compatible output latches. Despite the large number of on-chip comparators, the dissipation is less than 1 watt. For operation, it needs only voltage-reference and encode-signal circuitry, and a single −5.2-volt supply (Figure 2).

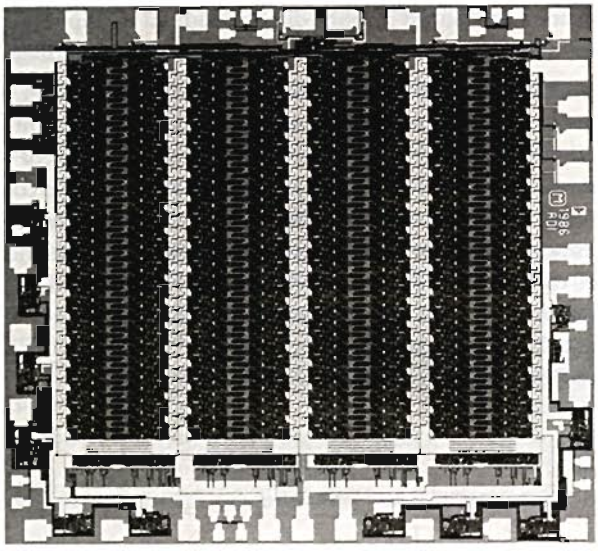
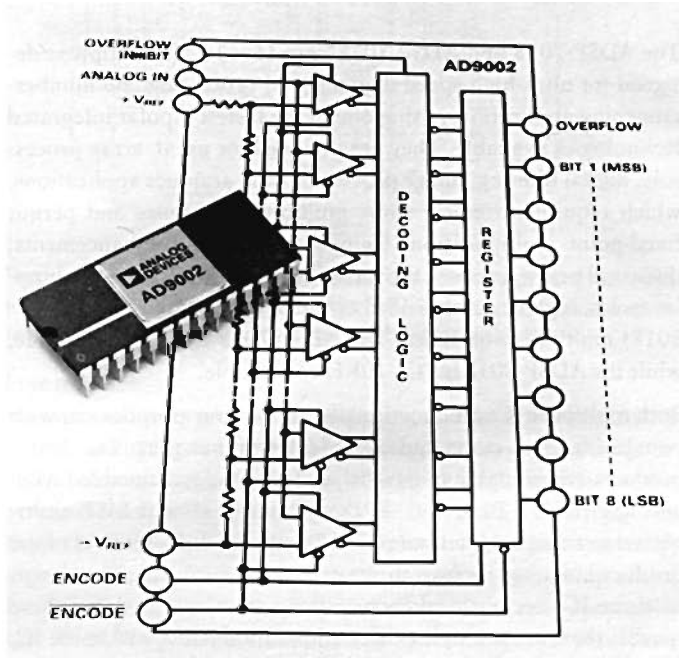


Figure 1. Die photograph illustrates chip density.

In addition to the excellent basic performance, the AD9002 has signal-to-noise of 46 dB (40 min) at 540 kHz, harmonic suppression of 63 dB at 1 MHz and 50 dB at 40 MHz, and maximum differential nonlinearity of ½ LSB. Two-tone intermodulation rejection (1 V p-p at 1.2 MHz and 1 V p-p at 2.4 MHz) is typically 60 dB.

Extra features include an external Hysteresis Control pin, which can be used to optimize converter sensitivity. An Overflow bit is provided, to indicate over-range input signals; if the function is not desired, it can be disabled by an Inhibit pin. The overflow bit also allows two AD9002s to be cascaded for 9-bit "flash" resolution without significant speed reduction.

*For technical data, use the reply card.



Two grades of the AD9002 are available (A or S, and B or T suffixes) with maximum nonlinearity of ¾ and ½ LSB, for either −25°C to +85°C (A/B industrial-temperature-range versions), or −55°C to +125°C (S/T MIL-STD-883C military versions). All grades are available in 28-pin ceramic DIPs; and S/T grades are also available in 28-pin LCCs. Prices (100s) start at $90 (AD9002AD).

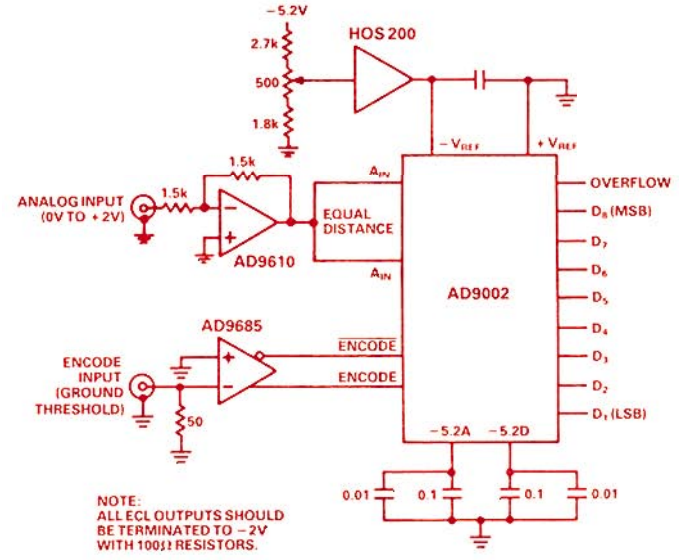


Figure 2. Typical application circuit, showing drive circuits for signal, reference, and encode command.

8-BIT, 300-MHz MONOLITHIC D/A CONVERTER FOR DISPLAYS

AD9703 Offers Speed and Design-In Simplicity with Low Glitch

Composite-Video Control Features Are On-Chip for up to 2K × 2K-Pixel Displays

by Tom Tice

The AD9703* is an ultra high-speed monolithic 8-bit video d/a converter (DAC) in a 24-pin DIP. Designed to be used in state-of-the-art high-resolution raster-scan video graphics systems, it offers ease of interfacing, high performance, high accuracy, low glitch, synchronized composite video functions, and guaranteed monotonicity. A complete video DAC solution for the raster-scan circuit designer, it includes a low temperature-coefficient voltage reference, input data latches, and synchronized video functions on chip. No external components are required to generate control signals which conform to the RS-170 standard. Performance specifications include an update rate greater than 300 MHz, a rise time of 1.2 ns, settling time of 6 ns, and glitch impulse of less than 45 pV-s (typical).

Its synchronized composite functions include Sync, Blank, Reference White, and 10% Bright. The reference-white input forces the analog output to the reference-white level, regardless of the data inputs; the 10% bright input can be used to generate a white cursor on a white background.

Designed primarily for use in raster-scan graphics displays, the AD9703 can easily handle the requirements for displays of 2,048 by 1,536 pixels and more, permitting the grey-scale level of this large number of pixels to be controlled at the required screen refresh rate. In addition to display, its low glitch and fast response also make it an excellent choice for waveform generation and other applications, such as radar displays, automated test equipment, and medical-imaging instrumentation.

Figure 1 is a block diagram of the AD9703. Its complementary binary inputs are emitter-coupled-logic-compatible (ECL, 10KH and 100K series). The video function inputs have individual internal registers, retaining full synchronization of the video functions with the system clock. This synchronization helps to prevent short or missing pixels. The strobe input to the AD9703 requires a differential ECL clock signal.

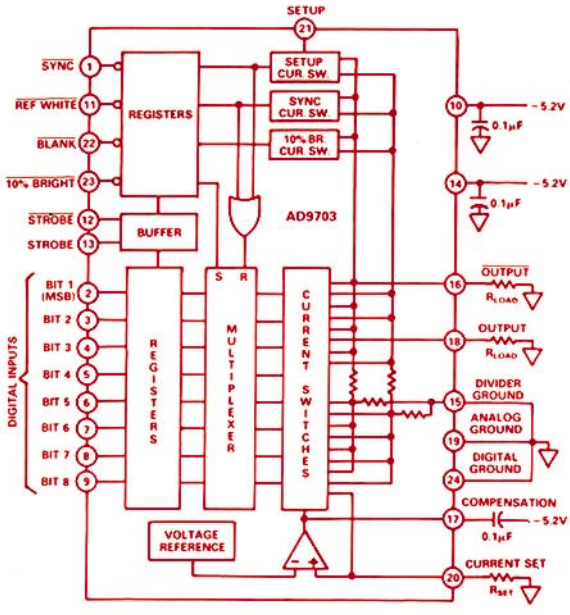
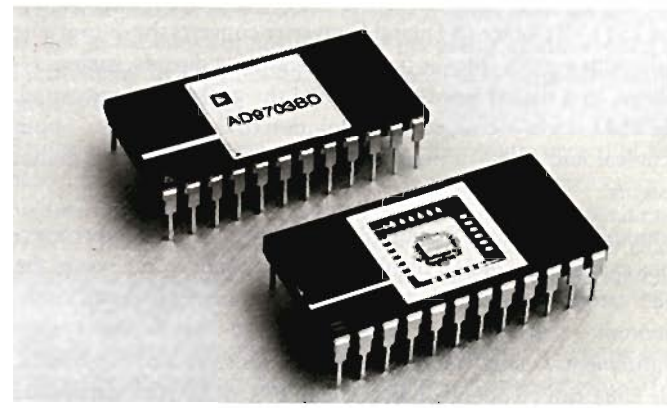


Figure 1. Block diagram of AD9703.



The DAC circuitry consists of two identical 4-bit binary-weighted current-sink DACs summed via a 16 to 1 resistive divider; settling time is fast and linearity is excellent. The current sources of the DAC are biased by the on-board control amplifier and the stable, highly regulated bandgap voltage reference. The user can adjust the full scale output current of the DAC by means of an external resistor, R_{SET}.

The AD9703 was designed to drive a doubly terminated 75-ohm cable (R_{LOAD}), equivalent to 37.5 ohms. The DAC provides a full-scale output voltage of −637.5 mV; thus, the LSB weight is 2.5 mV. The DAC is guaranteed to be monotonic, with differential and integral nonlinearity specified at less than ±0.2% of Gray Scale (full-scale output voltage); initial zero offset voltage is 2 mV.

The AD9703 has both true and complementary outputs for increased flexibility; they have internal impedance of 800 ohms and voltage compliance of −1.2V to +3V. The compliance range permits the user to shift the output voltage of the DAC to a level appropriate for the system. For example, in applications other than video, the full-scale voltage can be increased to any value within the constraints of the compliance specification.

The AD9703 requires but a single power supply voltage of −5.2V at 210 mA (typical), for a dissipation of 1.1 watts. If power is to be conserved, a −4.5V ECL standard supply can be used.

The chip includes the necessary circuitry to generate a complete composite video waveform, compatible with the RS-170 and RS-343 standards; functions included generate 10% bright, reference white, composite blanking, and composite sync levels, in addition to the DAC's 256 levels of gray. A setup pin of the IC can be connected in four ways to provide one of four commonly used setup values: 0 IRE, 7.5 IRE, 10 IRE, and 20 IRE.

The AD9703, housed in a 24-pin ceramic DIP package, is available for the industrial (−25 to +85°C) and military (−55 to +125°C) temperature ranges. It will soon be available screened to MIL-STD-883C. Prices (100s) start at $43.60 for the AD9730BW.

*Use the reply card for technical data.

FIRST MONOLITHIC RESOLVER-TO-DIGITAL CONVERTER

2S81 Resolver-to-Computer Interface Chip Provides 12-Bit Outputs

Accurate, Simple, Inexpensive, It Operates at Speeds up to 260 rev/sec, Has Velocity Output

by Richard Parker

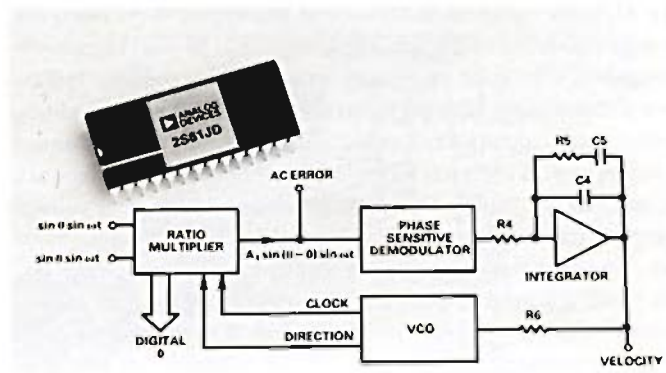
The 2S81* Resolver-to-Digital Converter converts the output sine and cosine signals from ac position-measuring devices, such as resolvers, to a digital word representing the angle being measured. The 2S81 is a low-cost, compact solution to the difficulties—both technical and cost—of interfacing resolver transducers to digital systems.

A monolithic IC in a 28-pin DIP, it provides 12-bit digital conversions at speeds up to 260 revolutions per second (rps). Users of the 2S81 can set the dynamic performance parameters—bandwidth, maximum tracking rate, and scaling—to match the system requirements, using standard low cost resistors and capacitors. The 2S81 can be operated with either TTL or CMOS, depending on the logic supply voltage (V_L); control inputs are TTL-compatible. The device's power requirement is only 300mW (maximum) at ±12 volts. It is manufactured using the Analog Devices proprietary BiMOS II process, which combines high-density, low-power CMOS logic with high-accuracy bipolar linear circuitry. Its price is $70 in 100s.

The need to determine a linear or rotary position occurs in the many applications where electronic systems are involved in the measurement or control of mechanical devices. For example, in controlled machining, the position of the cutting head relative to the workpiece must be known; in aircraft control, the angle of the control flap of an airplane wing must be measured.

This need to measure the rotary position of a shaft has increased tremendously with the increased use of electronic motor-control. The need to fully control brushless dc motors and have them follow required acceleration and torque profiles means that the control system must know, precisely, the angle of the shaft at all times. The choice of position transducer is critical; it must be reliable, rugged, and highly accurate. The resolver (and its close relative, the synchro) meets these needs; the resolver is basically an inductively coupled rotating transformer with a primary coil excited by an ac reference voltage at frequencies up to a few kilohertz. The coupled signal is picked up in the secondary coils, which are built in a fixed angular orientation to one another. The ratio of the magnitudes of the secondary signals is related to the absolute angle between the primary and secondaries.

Despite the advantages of synchros and resolvers as position and angle transducers, there are reasons why they haven't been used in many applications. The interface circuitry for these transducers is relatively complex. The relationship between the excitation signal and the two transducer outputs must be used to determine the corresponding angle information; only then can the angle signal be digitized. Until now, complex, costly, slow, and power-hungry modules or hybrids have been the only choice.



THE MONOLITHIC SOLUTION TO RESOLVER CONVERSION

Since the ratio of the magnitudes of the two resolver outputs (which represent the sine and cosine of the shaft angle) is a one-to-one mapping of the angular position, the best architecture to digitize these signals uses a ratiometric resolver/digital converter. The 2S81 circuitry provides tracking ratiometric conversion, which means that essentially continuous output position data is available without any conversion delay. Accuracy of the output value is 30 arc-minutes. The 2S81 design is inherently high in noise immunity, common-mode-voltage rejection, and tolerance of harmonic distortion in the ac signals.

In addition, the 2S81 provides a tachometric analog signal, proportional to the rotational speed of the shaft. This signal can replace the signal from the separate velocity transducer often used in position-control systems to provide loop stabilization and velocity-feedback data.

Connecting the 2S81 to the Resolver

The typical connection between the 2S81 and the resolver is shown in Figure 1. The signal from the reference oscillator energizes the primary winding of the resolver; in the 2S81, it is used to demodulate the resolver secondary signals.

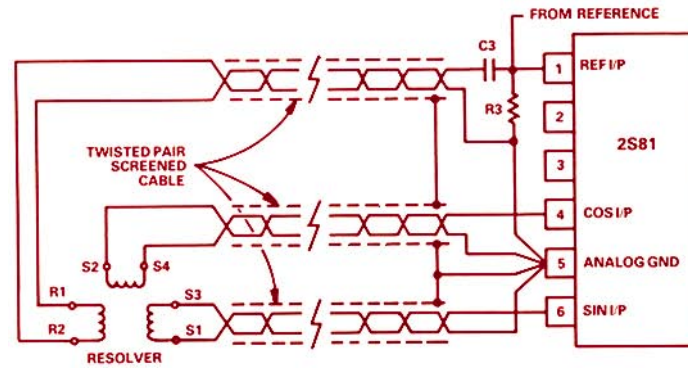


Figure 1. Connecting the 2S81 to a reference and a resolver.

*Use the reply card for technical data.

The reference requirements are not stringent. It can have a nominal value of 2 V rms and any frequency between 400 and 10,000 Hz. (The Analog Devices OSC1758* Hybrid Power Oscillator is specifically designed as a reference source.) Any excessive phase shift between the reference signal and the 2S81 input signals, which might degrade performance, can be corrected by adjusting the value of a resistance in the IC's external high-frequency filter.

The Digital Interface of the 2S81

The 2S81 is designed for easy interface to any microcomputer system (Figure 2). The digital output corresponding to the resolver position is available as 12 left-justified bits of data, appearing on an 8-bit bus in two bytes, selected by BYTE SELECT lines. One byte contains the eight MSBs of data; the second byte has four bits of data and four unused bits, in natural-binary number format. Either TTL or CMOS can be interfaced. There is no need for a conversion command; since the 2S81 is a tracking converter, it is always following the input (up to the maximum tracking rate), and conversion is automatically initiated by each LSB increment of the angle. A BUSY signal indicates when a conversion is in progress and the data bits are not valid. An INHIBIT input to the 2S81 prevents new conversion data from being transferred to the output latches while existing data is being read, without interrupting the tracking loop.

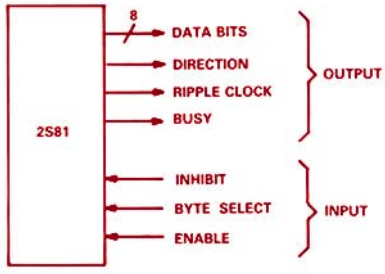


Figure 2. The digital interface of the 2S81 shows the inputs/output between the IC and the system bus.

The direction of input rotation is indicated by the DIRECTION logic output. A RIPPLE CLOCK output indicates each time the digital output of the converter passes through the major carry (all 1s to all 0s or the reverse), indicating that another revolution of the input transducer has been completed. This can be used directly for counting total revolutions.

The tachometric output, mentioned earlier, is a dc analog signal proportional to the rate of change, or speed, of the input angle. This output, which can be used directly as a control input or as an indicator on a display device, eliminates the need for a separate tachometer and its interface electronics.

OPERATION AND USER-ADJUSTABLE PARAMETERS

A functional block diagram of the 2S81 is shown in Figure 3. The ratio multiplier in the input section compares the inputs from the resolver with the most-recent angle (digital output value), which is generated by a 12-bit up-down counter. The counter is driven by a voltage-controlled oscillator (VCO), which in turn is driven by an integrator. The output of the ratio circuit goes to a phase-sensitive demodulator, using the resolver's reference; the dc output value—which becomes the input to the integrator—is proportional to the position error of the converter.

†Inductosyn is a trademark of Farrand Controls, Inc.

How the 2S81 works can be seen by considering two typical cases: for a *constant angle* (steady-state position—no counting), the VCO frequency must be zero, therefore its input must be zero; but since its input is from an integrator, the integrator's average input (i.e., the tracking error) must also be zero. For *constant velocity* (angle changing at a constant rate—counter counting at a constant rate), the VCO frequency must be constant, which can only happen if its input is constant, and *that* can happen only if the input to the integrator is zero—so the error is zero for constant velocity as well as for constant position. The integrator output is used as a tachometer signal, since it is proportional to velocity (depending on the VCO's linearity).

Besides offset adjustment and reference phase-shift correction, the design of the 2S81 allows the key performance parameters to be predetermined and set using calculated resistance and capacitance values. These parameters include input high-frequency filter characteristics, maximum tracking rate, and closed-loop bandwidth and transfer function.

High-frequency filtering is used to reduce the amount of noise present on the signal going to the 2S81's phase-sensitive detector. This noise is mostly due to noise on the signal inputs from the reference and resolver.

The maximum tracking rate of the 2S81 is 260 rps, but many applications don't need it. In order to minimize noise, the maximum tracking rate (VCO scale factor) should be set to match the expected input rate, like setting the range on an input amplifier to match the expected transducer output span.

The closed-loop bandwidth and dynamic performance of the tracking loop are important to the overall performance of the system in which the resolver and 2S81 are used. Two capacitors and a resistor can be used to adjust the loop's poles and zeros for desired response by tailoring the integrator's characteristics.

The 2S81 opens the way to expanded application of resolvers (and synchros and Inductosyns† as well), since it overcomes interfacing complexity, the major impediment to using these rugged, reliable, and accurate transducers. As a result of the low cost, compactness, and 12-bit performance of the 2S81, existing applications will benefit and new applications will develop rapidly, especially in electronic motor control.

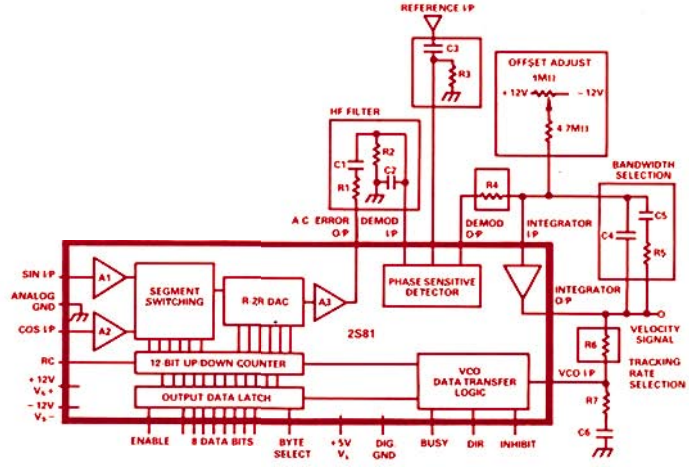


Figure 3. Functional block diagram of 2S81; note the external circuitry that enables the *user* to determine noise level, closed-loop dynamic performance, and maximum tracking rate.

MONOLITHIC PRECISION VOLTAGE REFERENCE

AD588BD Has ±1 mV Max Voltage Error, ±1.5 ppm/°C Max Drift

Kelvin Connections Minimize System Errors; Dual Outputs Are Available

by Bill Thompson

The AD588* is the first member of a new generation of monolithic precision voltage references. Long-time readers of this Journal will remember the 2.5-volt AD580 bandgap reference, introduced in 1974 [8-2 (12), 9-1 (6-7), 9-2 (20-21)] and the versatile pin-programmable bandgap AD584, introduced in 1978 [12-2, (6-7)]. The AD588 employs a stable, low-noise (patented) buried Zener-diode—laser-trimmed for both initial accuracy and low temperature coefficient. Used for many years—and thoroughly proven—in our d/a and a/d converters, it is now available in a 16-pin ceramic DIP for general-purpose applications.

It is the reference of choice for virtually all applications calling for 10 to 16 bits of absolute accuracy at reasonable cost. Examples include auto-calibration, systems that provide excitation for sensors (such as RTDs, strain gages, load cells, etc.), references for data-acquisition systems that include a/d and d/a converters, precision current sources, and power-supply controllers.

The AD588 (Figure 1) comprises a buried Zener-diode reference, a set of four low-drift high-gain (110 dB) feedback amplifiers (one services the Zener diode and the others provide sources, sinks, and returns for load currents)—and a network of thin-film resistors to provide the precision scaling for pin-programmable output-voltage ranges. By the choice of external jumper connections, fixed output voltages of +10.000 V, +5.000 V, ±5.000 V (tracking), −5.000 V, and −10.000 V are available.

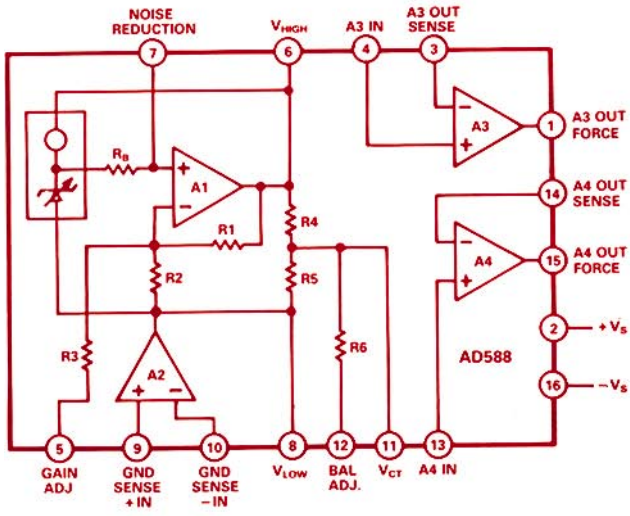
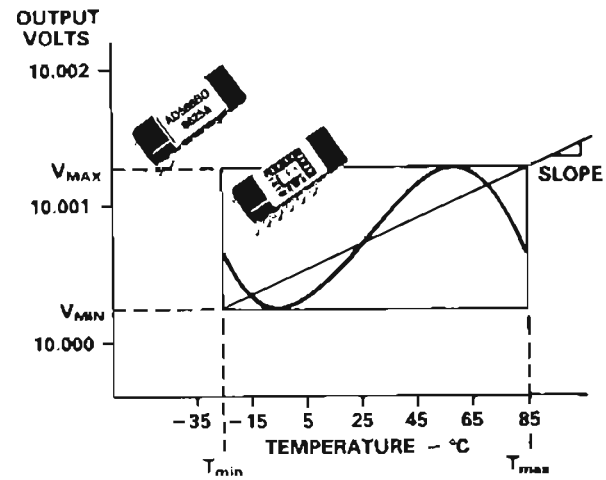


Figure 1. Functional block diagram of the AD588.

For the +10-volt connection, maximum error at +25°C is ±1 mV (0.01%) for grades B & C (±3 mV, or 0.03%, for A, S, and T); this allows the AD588 to be used as a ½-LSB (12-bit) system reference without any additional calibration or compensation. This low initial error, combined with a maximum temperature coefficient of ±1.5 ppm/°C (grades B and C, 0 to +70°C), rising to ±3 ppm/°C (grades A, B, C, −25°C to +85°C), permits the device to maintain its accuracy in an environment that is not

*For technical data, use the reply card.



temperature-controlled. The temperature coefficient is still only ±4 ppm/°C max for the S & T grades. Prices start at $12.75 in 100s (AD588AD).

AMPLIFIERS AND KELVIN CONNECTIONS

How the device works can be seen in Figure 2, where it is connected for +10-volt output; an auxiliary +5-volt output is also made available. Note first that the Zener diode is in series with a current source, which is driven from the output of A1; the lower end of the Zener is driven by the output of A2. Since A2 is a high-gain feedback amplifier, jumpered (8-10) as a follower, the low end of the Zener is driven to be equal to the input voltage to A2 (9), which is connected to the system ground point.

In the connection shown, the closed-loop gain of A1 is equal to $(1 + R_1/R_2)$, a laser-trimmed ratio that gives +10.000 volts at the output of A1. This output is buffered by jumpering it to the + input of A3 (6-4), and the output of A3 is jumpered to its negative input; in this follower connection, the output voltage at pin 1 must therefore be equal to +10.000 volts, referred to system ground.

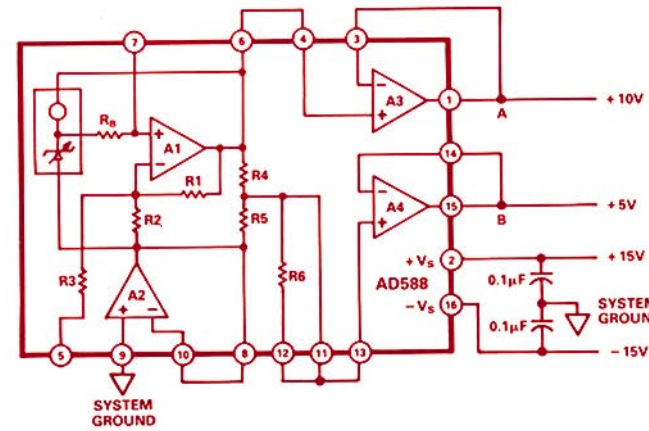


Figure 2. Connection for +10-volt (and +5-V) output.

Continuing, the output of A1 is connected to a 2:1 voltage divider ($R_4 = R_5$) and the jumpers across pins 11 and 12; they short out application resistor, R6, which is not needed here. This 5-volt auxiliary output is buffered by connecting it to the + input of A4 (13); like A3, A4 is fed back as a follower (14-15), so the output of A4 must be one-half of the output of A3, or about 5 volts, with respect to system ground.

Note that the closure of the feedback loops of A2, A3, and A4 through external jumpers makes it easy to use force-sense, or Kelvin, connections—a powerful technique for bringing accurate voltages to remote points despite a wide variety of possible impediments, such as series resistances, lead-thermocouples, etc., by simply closing the loop around them.

For example, if the resistance of the socket and lead between pin 1 and point "A" is 2 ohms, there will be a 20-millivolt (0.2%) drop when the rated load current of 10 mA is flowing through it. However, the feedback lead from "A" to pin 3 senses the load voltage (without drawing current), and amplifier A3 enforces the equality between A and the 10.000 volts from A1. The result is that the output of A3 will move up by 20 mV to service the voltage drop, but point A (pin 3) will remain at 10.000 V.

The same principle applies to connections to the second sensing point, at B (14), and to the system-ground sense connection, at pin 9. By changing the external connections, other output voltages can be programmed. For example, consider Figure 3, a circuit to provide +5 V and −5 V, with respect to system ground.

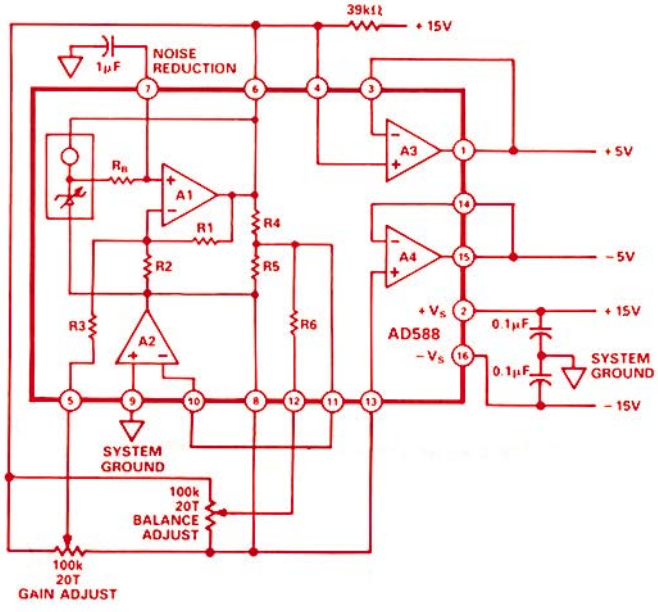


Figure 3. Connection for ±5-volt dual outputs.

In this case, the tap of the 2:1 10-volt R4-R5 divider is connected to the negative input of A2 (11-10), which draws negligible current. Since it must follow the voltage at system ground, the upper end must be at +5 volts and the lower end must be at −5 volts with respect to ground. These voltages are buffered by A3 (6-4) and A4 (8-13), respectively. In the ±5-volt connection, symmetry is maintained; both sides track to within ±0.75 mV (B grade). In the circuit shown, trim potentiometers may be provided for precise tweaking of gain (10.000 volts) and balance (±5.000 volts).

APPLICATION BRIEFS

The AD588 can be operated as a current source with the addition of a single external resistor. In Figure 4, an AD588 supplies a precision reference current to a 4-point probe assembly, used to measure the sheet resistance of semiconductor test patterns. In this case, A2 maintains 10 volts across control resistor, R_C, by sensing the voltage at its lower end (V_B) and keeping the lower end of the Zener diode at the same voltage, while the upper end of R_C is driven at $V_A = V_B + 10$ V. This forces a current of 10 V/R_C through the sample under test. The return current to ground is furnished by the output of A4, which servos probe point 3 to virtual ground potential, while the ground current flows through probe point 4 and the output of A4. The voltage from pickoff point 2 to ground, proportional to the sample's sheet resistance, is measured by a digital voltmeter. The trim potentiometer is used to calibrate the system with a sample having a known sheet resistance.

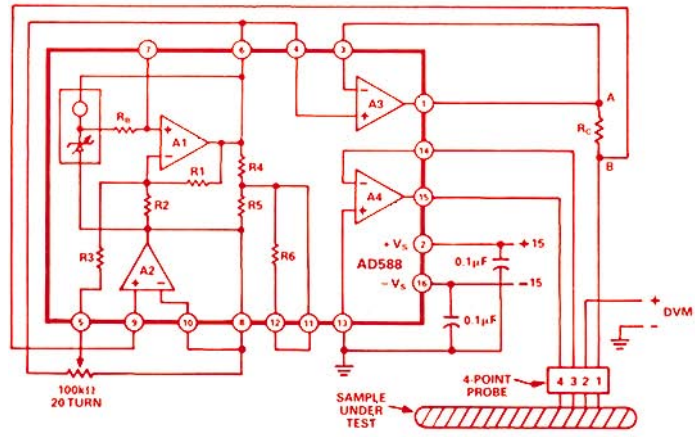


Figure 4. Current source for sheet-resistance measurements.

Because of its three-point sensing, the AD588 can also be used to excite a low-impedance bridge, using inside-the-loop current-boost transistors, while maintaining the common-mode voltage close to system ground without causing error current to flow. In Figure 5, the sense points, A and B, are driven at a 10-volt difference, while sense point, C, is held at ground potential by A2 (which draws negligible current). Q1 and Q2 provide a current-boosted output as required by the bridge impedance (for example, 40 mA to a 250-ohm bridge), but their V_{BE}s cause no error, since they're inside the loop. ◻

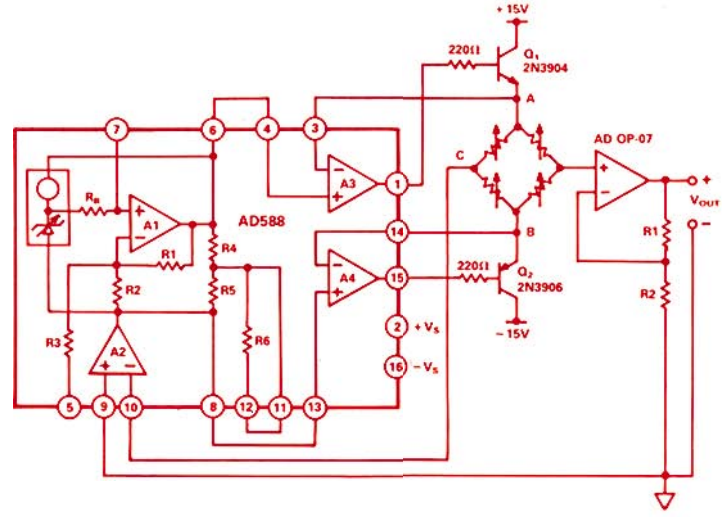


Figure 5. Floating bridge drive with minimum common-mode voltage.

QUAD 12-BIT READBACK DAC WITH 40-ns BUS-ACCESS TIME

AD392 Has Four Complete Double-Buffered Voltage-Output DACs

Has ± ½-LSB Max Linearity Error, Is Guaranteed Monotonic Over Temperature

by Bill Gotschewski

The AD392* (Figure 1) consists of four complete double-buffered 12-bit voltage-output DACs in a single 32-pin hermetically sealed package; it has a readback capability that can be used to verify that the data latched into the DAC registers is the same as the data sent from the microprocessor, a key feature in applications such as automatic testing and robotics. Its fast 40-nanosecond bus-access time (guaranteed over the temperature range) ensures that the device can interface with high-speed microprocessors operating at speeds beyond 20 MHz without needing Wait states.

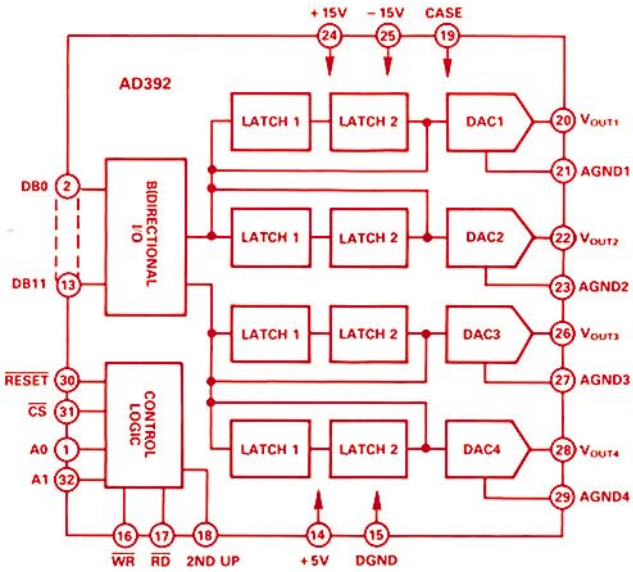
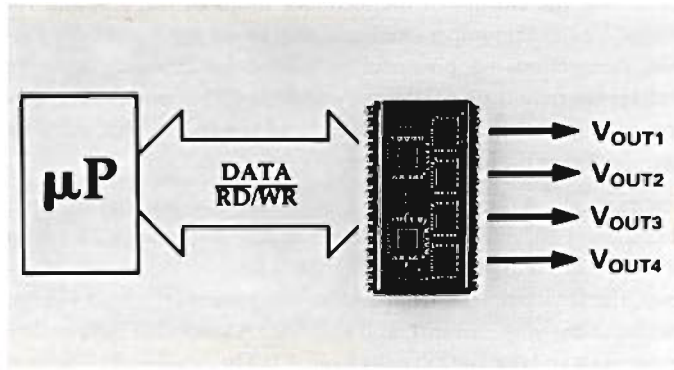


Figure 1. Block diagram of the AD392 quad DAC, showing four complete DACs, double buffering, and bidirectional I/O.

Each DAC is complete on a monolithic chip, with current-steering switches, a laser-trimmed resistance-ladder network, precision output amplifier, stable voltage reference, and double-buffered inputs. The bidirectional I/O and control logic are furnished on a pair of proprietary gate-array chips.

Integral linearity error is guaranteed at ± ½ LSB maximum, and differential linearity is ± 1 LSB max; the AD392 is monotonic over the 0°C to +70°C operating temperature range. In addition to the fast digital bus-access time, its analog outputs settle to within ± ½ LSB in a maximum of 4 microseconds (Figure 2). The AD392 is complete, with its control logic, registers, latches, and the four DACs; it needs only a ± 15-volt supply for operation. The hermetic pin-stake packaging technique results in a low price of $99 in 100s.

Where are quad readback dacs useful? Besides ATE and robotics, the AD392 is ideal for systems requiring digital control of many



analog voltages and for the monitoring of the DAC inputs, especially where board space is at a premium. Besides serving as a check to confirm that the data put on the bus has actually reached a DAC's physical input, the readback feature allows each DAC's register to do double duty as a memory location for the most recent value of its output variable.

The individual DAC registers are accessed by address lines, A0 and A1, and control lines, $\overline{CS}$ and 2ND UP. These control signals permit the registers of the four DACs to be loaded sequentially and the outputs to be updated simultaneously.

There are a number of other useful conveniences; for example, each DAC is independently addressable, providing a versatile control architecture for simple interface to microprocessors; the readback can drive 2 TTL loads, so external buffering is not needed. An asynchronous automatic Reset can be used to set all DACs to zero volts simultaneously at any time, a useful feature for system calibration or—in ATE—when a new round of tests requires that all DAC outputs must be cleared. Laser trimming at the factory ensures the linearity specifications and makes external trim potentiometers unnecessary. Dynamically, digital-to-analog glitch impulse is only 2 mV-µs and crosstalk is 0.1 LSB.

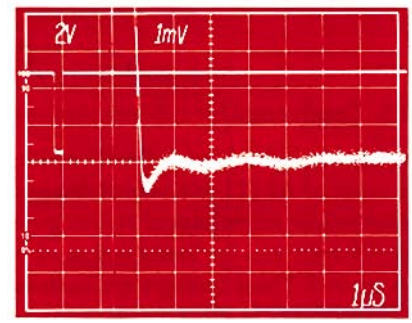


Figure 2. Output-voltage settling time (20-volt step).

*Use the reply card for technical data.

NEW DSP ICs FOR INCREASED FUNCTIONALITY & PERFORMANCE

Integer Arithmetic Unit; 5-Port Register File; Floating-Point Chip Sets; 24 × 24 Multiplier; Single-Port MAC; for High Speed, Low Power, Low Chip Count

by Bill Schweber

Since Analog Devices introduced the first low-power CMOS Digital Signal Processing (DSP) integrated circuits in 1983 [see *Analog Dialogue* 17-1], the applications of DSP have grown tremendously. Wherever there has been a need for rapid processing of data, especially from real-world phenomena, integrated circuits that perform number-crunching operations in hardware have provided an opportunity to analyze and explore information in new ways. Diverse applications, such as fast-Fourier-transform (FFT) waveform analysis, voice recognition, correlation, digital filtering, sonar signature-analysis, pattern recognition, and computer graphics displays—all have benefited from the capabilities of systems based on DSP components.

This growth owes much to increased functionality and speed, reduced costs, and an increase in designers' understanding of what DSP can do. At the same time, the number and versatility of the DSP components from manufacturers such as Analog Devices has increased, providing additional impetus for a widening of the spectrum of applications. Prominent features of ADI's entries include high speed, innovative architectures, and low power consumption. Advanced technologies, such as high-speed-low-power CMOS and ultra-high-speed bipolar processes have been used to obtain maximum performance. Figure 1 plots cycle time against resolution for a sampling of our DSP product line as of mid-1987.

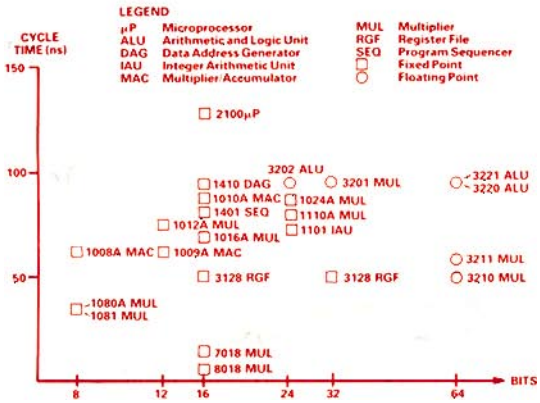


Figure 1. DSP and number-crunching components from Analog Devices embrace a wide range of functionality, resolution, and speed for the spectrum of applications.

The DSP family now encompasses a large array of products, ranging from *number crunchers*: fixed- and floating-point multipliers, multiplier/accumulators (MACs), and arithmetic and logic units (ALUs); and *system-integration chips*: address generators, program sequencers, and register files for Word-Slice™ systems); to the unique ADSP-2100 *single-chip microprocessor*.

A typical DSP system architecture (Figure 2) requires an assemblage of these to provide the all the necessary computation and control functions. *Fixed-point components* perform arithmetic and logical operations, using number formats such as twos-complement or unsigned-magnitude representations. Accumulators sum data and products with previous results—an essential operation in most DSP algorithms. Although fixed point is restrictive, fixed-point ICs offer speed, simplicity, and low cost; they are ideal for certain dedicated applications; scaling and other manipulations such as *block floating point* can be handled with shifting and format selections provided by the ICs.

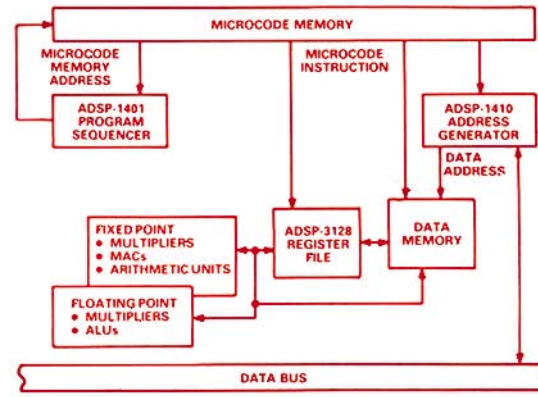


Figure 2. Functional block diagram of a typical Word-Slice™ system; it can use a wide variety of DSP components.

Floating-point components are intended to handle a wider dynamic range of numbers more easily, using multipliers and arithmetic-and-logic units (ALUs). Depending on the application, single-precision (32-bit) or double precision (64-bit) floating point representation may be needed. Analog Devices Word-Slice program sequencers, address generators, and register files act as *management and support* components for the multipliers, multiplier/accumulators, and ALUs.

The recently introduced ADSP-2100 is a complete digital signal processing microprocessor in a single IC (*Analog Dialogue* 20-2) for applications where low package count and software flexibility are needed. It integrates computational units, data-address generators, and a program sequencer with an instruction cache in a 100-pin grid-array package.

In the following pages, some recently available DSP ICs are introduced. They are not restricted to any one aspect of DSP systems; indeed, they increase performance and functionality in all key segments of the overall DSP family. They include:

- **ADSP-1101 Integer Arithmetic Unit** (2.4 ms for a complex 1,024-point fast Fourier-transform)—page 16
- **ADSP-3128 Five-Port Register File** (provides fast scratchpad memory)—page 17
- **ADSP-3211/3221/3201/3202 Floating-Point Number-Crunchers** (to 20 MFLOPS single-precision and 5 MFLOPS double-precision multiplication, and 10 MFLOPS ALU)—pages 18-19
- **ADSP-1024A 24 × 24-Bit Multiplier** (computes in 95 ns, makes floating-point unnecessary for many applications)—page 20.
- **ADSP-1110A Single-Port Multiplier-Accumulator** (minimizes connections, processes at speeds comparable to many 3-port entities)—page 21.

NEW DSP ICs FOR INCREASED FUNCTIONALITY & PERFORMANCE

High-Speed Integer Arithmetic Chip Combines Numeric Operations

ADSP-1101 Can Compute 1,024-Point Complex FFT in 2.4 Milliseconds

The ADSP-1101* Integer Arithmetic Unit is a powerful single-chip IC that offers high speed (80ns max cycle time) and a high level of integration for complex integer operations without external logic. These functions make it feasible to compute a 1,024-point complex fast Fourier transform (FFT) in 2.4 ms (Figure 3):

- 16 × 16-bit array multiplier
- 40-bit adder-subtractor
- logic unit
- dual 40-bit accumulators
- shifter logic
- block floating-point control circuitry.

The architecture and performance of the ADSP-1101 suit it ideally for digital filters and FFTs. Units can be physically cascaded to perform single-cycle FIR (finite impulse-response) filters without additional memory or other hardware. The ADSP-1101 simplifies FFTs by performing six-cycle radix-2 butterfly operations entirely on chip. Fast function generation (e.g., using Taylor/Chebyshev series) can also be performed on-chip.

INTERNAL DESIGN

The ADSP-1101 has two 16-bit input ports and a 20-bit output port. Up to six 16-bit words can be transferred through the three data ports in a single cycle. The user can choose the manner of loading of the input registers and preloading of the accumulators.

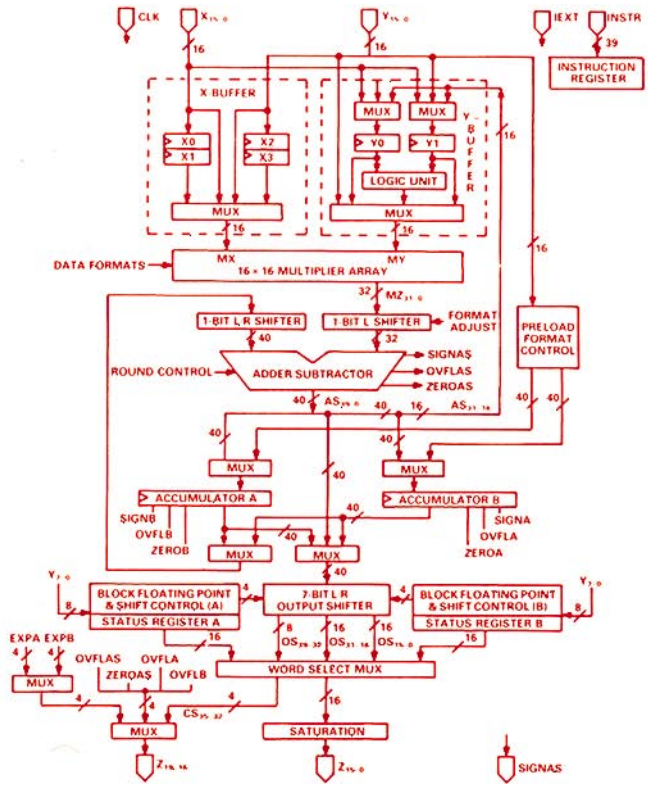
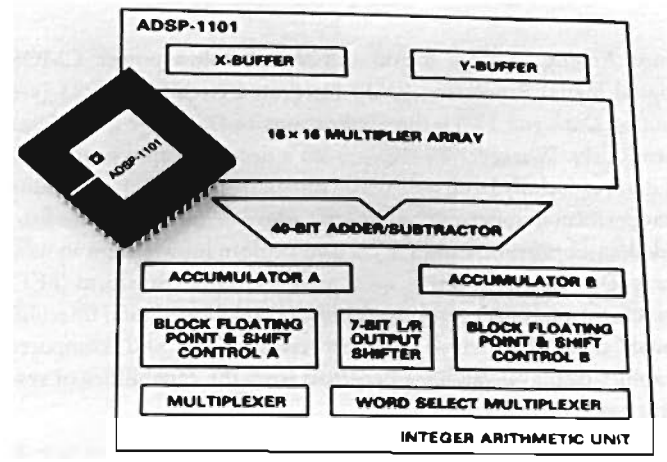


Figure 3. Functional block diagram of ADSP-1101.

*Use the reply card for technical data.



The 39-bit instruction word is divided into subfields that allow independent control of the various functional elements, in a highly orthogonal instruction set. If all the flexibility of the ADSP-1101 is not required, the pins for fixed instructions can be connected to either +5 V or ground to reduce the width of the instruction word coming from the microcode memory.

The 16-bit X port and Y port provide incoming data to the input data-buffers. The X buffer consists of four 16-bit registers, two feedthrough paths, and a multiplexer. The Y buffer has two 16-bit registers, a feedthrough path, the logic unit, and three muxes.

Formatting is quite flexible. The Integer Arithmetic Unit can process twos-complement, unsigned-magnitude, or mixed-mode fixed-point data in multiplication operations. An implied binary point can be implemented wherever desired. Saturation can be used in the event of overflows. The ADSP-1101 also has the quasi floating-point ability to autonormalize a single datum output from a selected accumulator. The autonormalization handles both twos-complement and unsigned-magnitude numbers by shifting them up to 7 bit-positions to left or right. The normalized exponent is available in the output register, along with the data bits.

For many computations, true floating point is unnecessary, unwieldy, and slow. In integer computations, *block floating-point* (BFP) is used to prevent overflow and preserve precision in applications requiring extensive iterative computation; problems include either an overflow of the fixed-point data fields as results grow in magnitude or a loss of precision as the results decrease. The ADSP-1101 chip contains all the control circuitry needed to implement block floating-point, by scaling a block of fixed-point data by a common exponent, keyed to the block's largest element. BFP is most useful when algorithms can be structured in multiple stages, as in FFTs, infinite impulse-response (IIR) filters, and some matrix operations.

The ADSP-1101 is fabricated with the Analog Devices high-speed, low-power 1.5-micron CMOS process, which results in a 70-ns (max) cycle time and low power dissipation (375 mW max). The ADSP-1101 is available in a 100-pin grid array. Prices start at $88 in 100s.

Multiport Register File Speeds DSP Systems, Reduces Chip Count

ADSP-3128 Scratchpad Memory Is Configurable, Can Be Cascaded for Expansion

The ADSP-3128* single-chip Multiport Register File is designed to function as a scratchpad memory for fast arithmetic processors, such as the multipliers and ALUs available from Analog Devices. It has an internal RAM, which can be accessed through two 16-bit input ports, two 16-bit output ports, and one bidirectional 16-bit data port. The internal RAM can be configured as 128 × 16 bits or 64 × 32 bits.

By eliminating the machine cycles wasted in transferring data, the ADSP-3128 Register File assists high-speed, fixed- or floating point DSP ICs to operate at their full computational speed. This single IC substitutes for the dozen or more discrete ICs and high-speed RAMS required to build a register file, while saving board space and power, and eliminating off-chip time delays. The ADSP-3128K has a 22-ns clock-to-valid output delay, and 35-ns address-to-valid output delay in the transparent mode. Additional ADSP-3128s can be used to expand memory space for more bits per data word (side by side) or for more data words.

The Multiport Register File is basically a high-speed static RAM, surrounded by the latches and control logic needed to simplify interfacing (Figure 4). Six internal *data* paths, all 32 bits wide, connect this RAM with multiplexers (muxes) and latches. Of the six data paths, there are three Reads and three Writes. There are also three 8-bit internal *address* paths that connect the RAM with muxes and address latches, with corresponding Chip Selects time-multiplexed to allow the presentation of up to six 7-bit addresses to the RAM per cycle. As a result, up to six RAM reads/writes are possible per cycle, using high and low levels.

The memory configuration of the ADSP-3128 can be dynamically programmed. This allows the IC to be used for 16-bit fixed point,

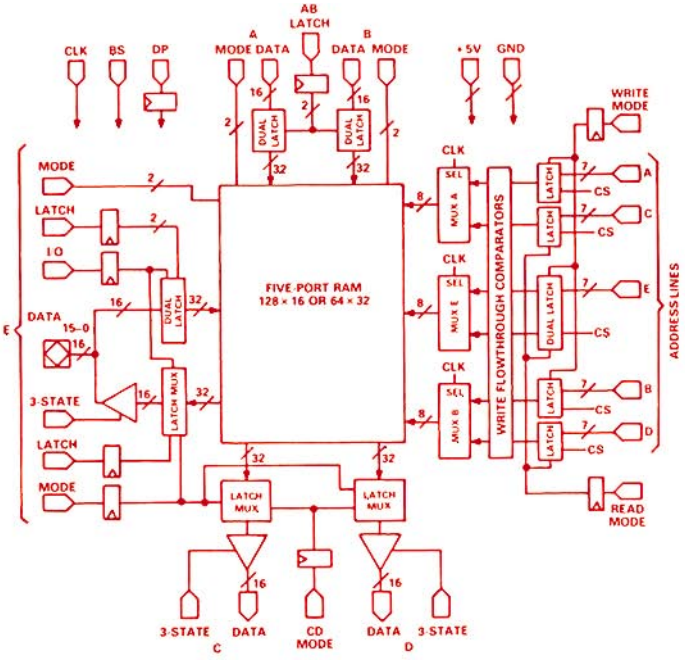
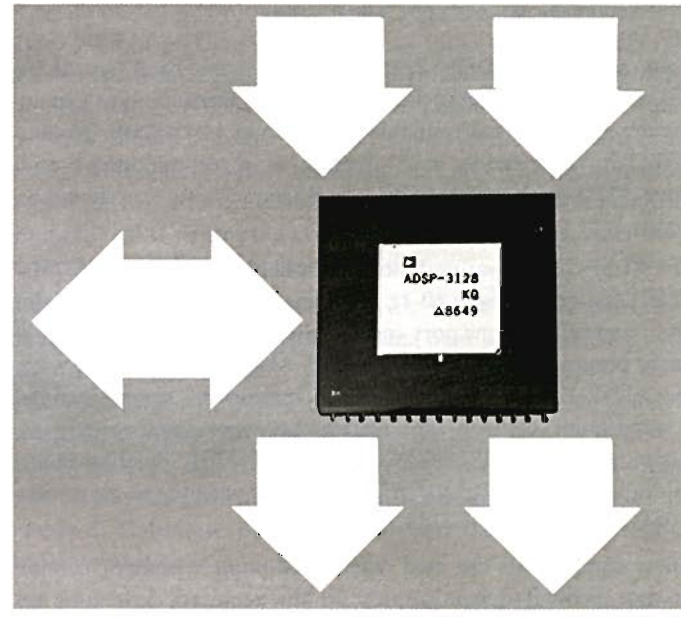


Figure 4. Functional block diagram of the ADSP-3128.

*Use the reply card for technical data.



32-bit fixed point, single-precision 32-bit floating point, or double-precision 64-bit operation, as needed at different points in the process of executing the system's microcode.

To accommodate critical system timing requirements, the ADSP-3128 provides a variety of latching modes (i.e., latching on clock HI, latching on clock LO, or remaining transparent) for both the data and address ports. For example, the write-data ports, A, B, and E, have control lines that define the input-data latching mode for the single-precision 128 × 16 configuration (16-bit data to one of 128 addresses). Similar modes are available for the read-data ports, C, D, and E; and other modes are available for the double-precision 64 × 32 configuration, such as: write A data to the most-significant half (of 32-bit addressed space) on HI, and write B data to the least-significant half on LO.

Each write-data port has an independent write-flowthrough control that can pass data through the register file without a pipeline delay; for instance, data is written to RAM via A and read from RAM via C in the same clock LO phase (transparent mode). Register-to-register transfers are also handled in two clock phases in similar fashion. The 7-bit addressing latches of the write (A, B, E) and read (C, D, E) ports also have various modes, to allow addresses to become valid on clock HI (write), clock's rising edge (read), or transparently (flowthrough).

The ADSP-3128 provides the potential for highest performance in a DSP system. In the single-precision mode, up to six 16-bit data transfers per cycle are attainable. The double-precision mode allows up to five 32-bit data transfers per cycle, for a total data rate ("bandwidth") of 160 bits/cycle. This speed insures that the Multiport Register File meets the needs of many applications for high-speed temporary data storage. The device, which uses a low-power TTL-compatible CMOS fabrication process, dissipates 1.75W maximum. The ADSP-3128 is packaged in a 144-lead pin-grid array. Prices start at $145 in 100s.

NEW DSP ICs FOR INCREASED FUNCTIONALITY & PERFORMANCE

High-Speed Floating-Point Multipliers and ALUs Follow IEEE Standard 754

ADSP-3211—Up to 64-Bit Multiplication; ADSP-3201 – 32-Bit Version

ADSP-3221—64-Bit ALU with Increased Instruction Set; ADSP-3202 – 32-Bit Version

Two multipliers (ADSP-3211* and ADSP-3201*) and two ALUs (ADSP-3221* and ADSP-3202*) have been introduced to extend the range of functions available from among ADI's floating-point DSP ICs. This family now consists of three multipliers and three ALUs, with major architectural characteristics as shown in Figure 5.

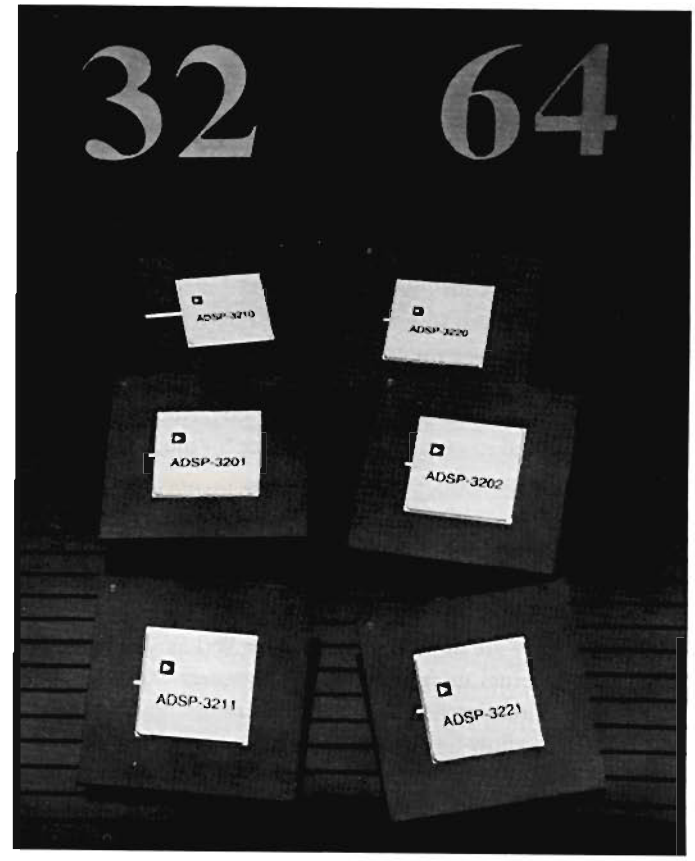
The ADSP-3211 Floating-Point Multiplier is similar to the ADSP-3210 (*Analog Dialogue* 20-1), but it has two input ports and eight input registers (vs. one port and 4 registers) for faster loading and easier programming. The ADSP-3221 ALU, pin-compatible with the ADSP-3220 ALU, extends the instruction set to include floating-point division and square-root operations exactly as recommended by IEEE-754. The ADSP-3201 Floating-Point Multiplier and ADSP-3202 ALU are 32-bit versions of the 64-bit ADSP-3211 and ADSP-3221.

These components are used when fixed-point arithmetic cannot provide enough dynamic range in the required cycle time or is in some other way inadequate for the application. They form the basic elements of a single- or double-precision high-speed digital signal processor with wide dynamic range and low power dissipation.

Both multiplier and ALU pairs can be dynamically programmed for either fixed- or floating-point operation, thus offering the desirable possibility of using an optimal combination of floating- and fixed-point operation within a given set of computations. Engineering work stations, minicomputers, and array processors require the wide dynamic range of *64-bit, double-precision* operations for applications such as SPICE simulation and finite-element analysis. High speed *32-bit single precision floating-point* is often sufficient for sonar, radar, and guidance system signal processing. *Fixed-point 32-bit* arithmetic is typically employed in graphics systems to calculate memory pointers to pixel arrays.

The ADSP-3211 Multiplier and ADSP-3221 ALU support four data formats: 32-bit single-precision and 64-bit double-precision floating point, as well as 32-bit unsigned and twos-complement fixed point.

The ADSP-3201 Multiplier and ADSP-3202 ALU are pin-compatible with the ADSP-3211 and ADSP-3221 but provide 32-bit formats only. All ICs support IEEE Standard 754 for single- and double-precision floating-point format (summarized in Figure 6†) and operations. The multiplier and ALU would be used with other microcoded components, such as a program sequencer (e.g., the ADSP-1401), microcode program memory, a data-address generator (e.g., the ADSP-1410), and data memory. Either multiplier can be used with either ALU, depending on system requirements. The multipliers/ALUs provide multiplication at up to 20 MFLOPS single-precision and 10 MFLOPS double-precision, with a 10 MFLOPS ALU.



The high-speed design of these multipliers and ALUs uses a single internal pipeline stage to achieve high throughput while simplifying programming. This minimal internal pipelining results in low latency, which is important in many scalar operations. All chips are fabricated in 1.5-micron CMOS, and each consumes less than 750mW maximum, using a single +5-volt supply.

MULTIPLIERS

PART NO.	WORD LENGTH	INPUT PORTS	INPUT REGISTERS	PGA LEADS	FUNCTION
ADSP-3210	64 Bits	1	4	100	Basic Multiplier
ADSP-3211	64 Bits	2	8	144	Adds Unsigned-Magnitude & Mixed-Mode Fixed-Point Multiplication
ADSP-3201	32 Bits	2	8	144	Pin-Compatible with ADSP-3221; 32-Bit Operation Compatible

ALUs

PART NO.	WORD LENGTH	INPUT PORTS	INPUT REGISTERS	PGA LEADS	FUNCTION
ADSP-3220	64 Bits	2	8	144	Basic ALU
ADSP-3221	64 Bits	2	8	144	Pin-Compatible with ADSP-3220; Adds Exact IEEE Floating-Point Division; Square-Root Operation
ADSP-3202	32 Bits	2	8	144	Pin Compatible with ADSP-3221; 32-Bit Operation Compatible

Figure 5. Comparative features of floating-point ICs, including the four devices introduced here.

*Use the reply card for technical data.

†A discussion of floating-point formats can be found in *Analog Dialogue* 20-1, page 8.

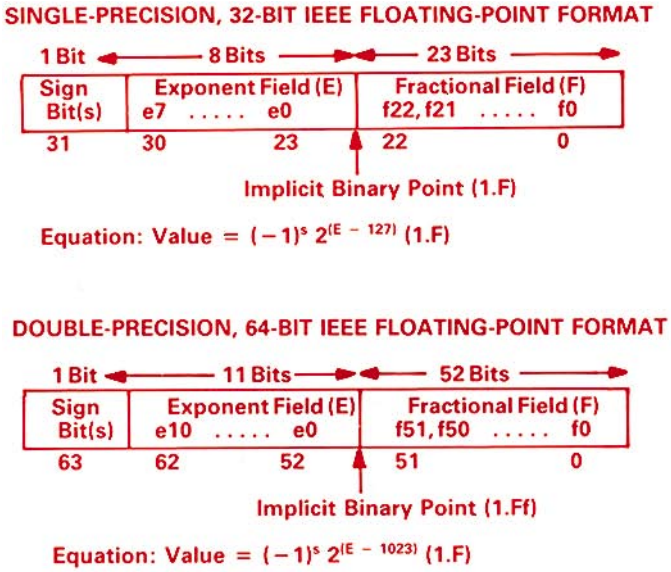


Figure 6. IEEE-754 floating-point-number formats for 32 and 64 bits.

MULTIPLIER AND ALU OPERATION

A block diagram of the ADSP-3211 multiplier IC is shown in Figure 7. (The ADSP-3201 is essentially the same, but with 32-bit formats only). Figure 8 is a block diagram of the pin-compatible ADSP-3221/3220/3202 ALUs. The multipliers and ALUs share a common form of operation: all input data is loaded into a set of input registers with both the rising and falling clock edges. At the end of the first processing cycle, partial results and most control lines are clocked into a set of internal pipeline registers. In most operations, processing concludes with the second clock cycle, at which time results are clocked into the output register. An output multiplexer allows both the LSP and MSP of a 64-bit fixed-point multiplication to be outputted to the system bus through the 32-bit output port in a single output cycle.

Operations can be overlapped where required, because there is a single level of pipeline register, and all input and output data is stored in internal registers. All input registers have their own independent load controls, so the same data can be loaded to multiple registers simultaneously. Control signals are supplied to the devices at the cycle rate of the multipliers and ALUs; this avoids a need for the sequencing-control cycle time to be faster than the multiplier/ALU processing cycle rate. As a result, less expensive, slower microcode memory can be used.

Because these devices conform with the IEEE standard for floating-point numbers, algorithms that have been developed and tested on other computers can be ported over to these ICs with high confidence. The four rounding modes of the standard—rounding to nearest number, to plus infinity, to zero, or to minus infinity—can be selected for any number format. External status pins on the ICs show five exception conditions described in the standard: underflow, overflow, invalid operation, inexact result, and division by zero.

All four ICs are available in 144-pin grid-array packages. Selections are available for 0 to +70°C and −55°C to +125°C operation, and 50-ns and 60-ns clock cycles (3211 and 3210 L-grade, respectively), as well as processing to MIL-STD-883C. Prices (100s) for the ADSP-3211, -3201, -3221, and -3202 begin at $300, $97, $300, and $97.

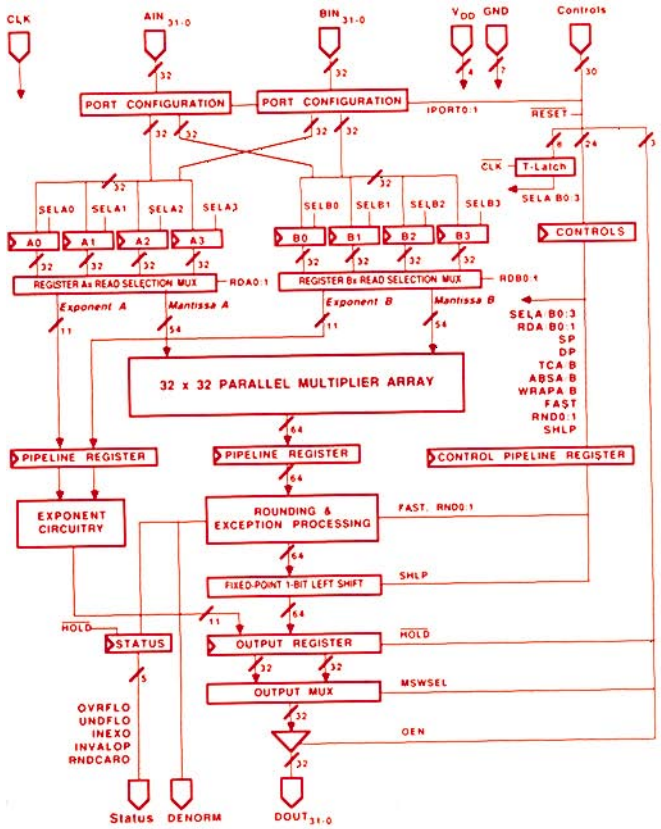


Figure 7. Functional block diagram of the ADSP-3211 floating-point multiplier.

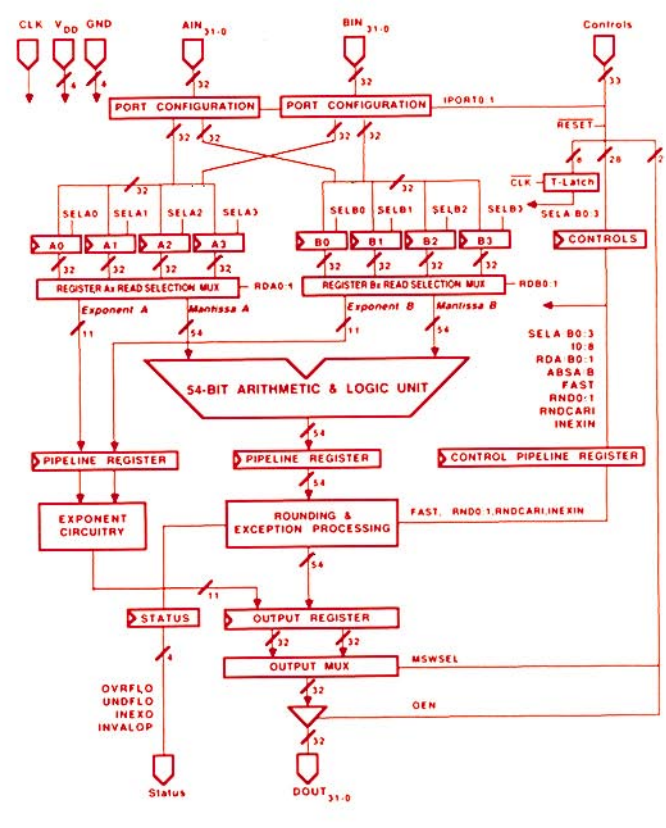


Figure 8. Functional block diagram of the floating-point ALU.

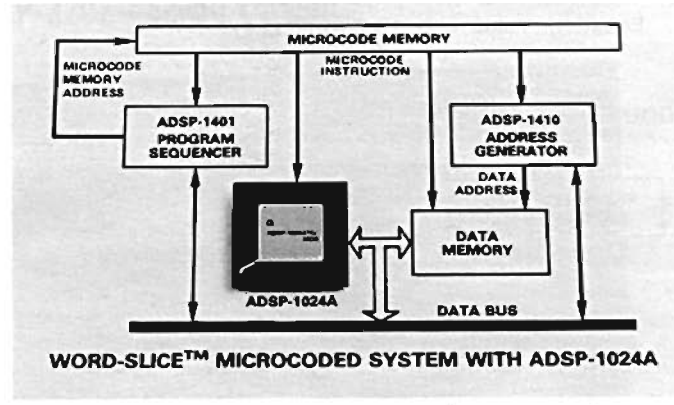
High-Speed 24 × 24-Bit Multiplier Performs Computation in 95 ns
CMOS ADSP-1024A Provides Rounding and Shifting Options, Status Flags

The ADSP-1024A is a high speed, low power 24 × 24-bit parallel multiplier characterized by a maximum multiply time of 95 nanoseconds. Fabricated in 1.5-micron CMOS, it is a twice-as-fast pin-for-pin replacement for the ADSP-1024 (Analog Dialogue 19-1). The ADSP-1024A is intended for digital signal-processing applications, such as digital filtering, Fourier transformations, correlation, voice recognition, and mantissa multiplication (in floating-point operations).

The 24-bit operation of the ADSP-1024A is needed when existing 8, 12, or 16-bit multipliers have insufficient coefficient accuracy or produce too much digital noise, especially in applications where there are many intermediate calculations. If it were not available, designers would have to choose between double-precision operations with 12- or 16-bit multipliers, designs using paralleled multipliers, 32-bit fixed-point multipliers, or floating-point ICs. These approaches are often more costly than using the ADSP-1024A and/or have slower cycle times for complete multiplications.

The ADSP-1024A is a three-port device with two 24-bit input ports and one 24-bit output port (Figure 9). The 48-bit output product is generated as two 24-bit products, the LSP and MSP (Least Significant and Most Significant Product) which share the single output port. Both the MSP and the LSP can be transferred out in a single cycle. Input data is in twos-complement format. If only a 24-bit product is desired, the 48-bit result, also in twos complement, can be left-shifted and rounded by control lines that can cause a 1 to be added to either bit 23, 22, or 21 of the LSP.

The input and output registers are D-type positive-edge-triggered flip-flops. The two input registers are controlled by independent clock lines. A third clock line is used to control the product registers. Each of the 24-bit product registers has its own three-state output control. The three-state outputs and independently clocked inputs allow the ADSP-1024A to be connected directly to a single 24-bit bus. Left-shift is available for either the LSP or the MSP (or both) outputs.



WORD-SLICE™ MICROCODED SYSTEM WITH ADSP-1024A

Flag bits (Figure 10) indicate overflow and normalized product output; they are used to check output range and determine what shift option can be used. In twos-complement multiplication, at least two redundant sign bits will be produced, except for the product of two full-scale negative inputs. In that case, the Overflow flag (OVF) will be set. For all other cases, a left-shift can be used to eliminate a redundant sign bit and gain one bit of magnitude information (shifted in from the LSP). If the multiplication result is small, there will be additional redundant bits; at least one more of these can be eliminated by an additional left-shift to improve resolution in the MSP. If this would cause error because the most-significant magnitude bit and the sign bit differ, NORM shows that the output is already normalized and another left shift would destroy the sign bit.

The ADSP-1024A is packaged in a ceramic 84-pin grid-array (PGA) package and dissipates 450 milliwatts. Four grades of the multiplier are available. The J/K grades are specified from 0°C to +70°C with maximum multiply times of 120/95 ns; S/T are specified over the full −55°C to +125°C military temperature range (MIL-STD-883C processing is available), with maximum multiply times of 150/120 ns. Prices start at $81 (J grade, 100s).

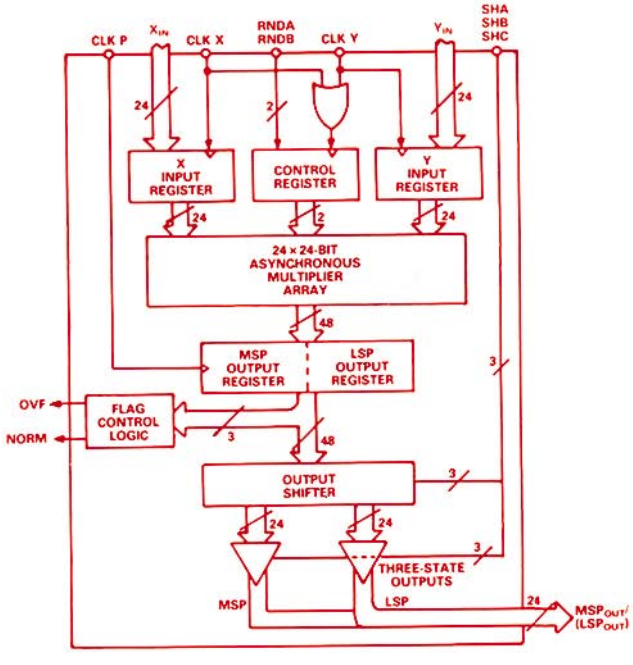


Figure 9. ADSP-1024A functional block diagram.

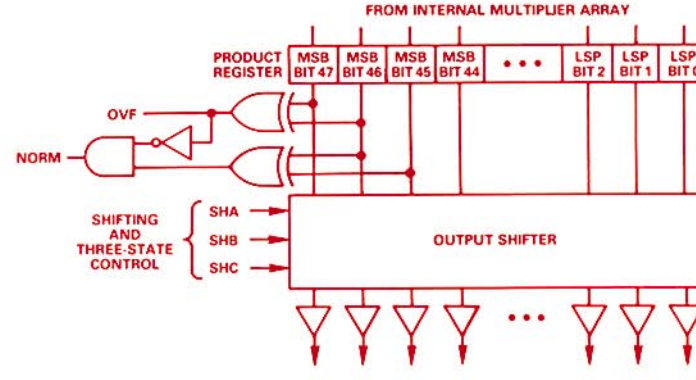


Figure 10. Flag and shift logic.

NEW DSP ICs FOR INCREASED FUNCTIONALITY & PERFORMANCE

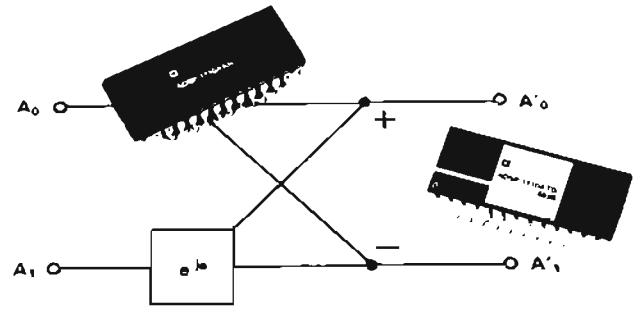
Single-Port Multiplier/Accumulator in a 28-Pin, Low-Cost Plastic DIP

ADSP-1110A: 16 × 16 Multiply-Accumulate in 85 Nanoseconds

The ADSP-1110A* is a high-speed, low-power 16 × 16-bit multiplier/accumulator (MAC) that, at 85 ns, is 125% faster than its predecessor, the ADSP-1110 (*Analog Dialogue* 18-2). Its single-port design offers processing power comparable to three-port MACs, but in a low-cost, space-saving package. In a 28-pin PLCC, the ADSP-1110A is industry's smallest 16-bit MAC. The ADSP-1110A contains two 16-bit input registers, a 16 × 16-bit multiplier, and a 40-bit accumulator. It operates on a standard +5-volt supply and is TTL compatible; the 1.5 micron double-metal CMOS process provides speed with a low power dissipation of 250 mW max. It is ideally suited for the basic DSP tasks, which are characterized by repeated multiply-add, such as filtering, FFTs, correlation, matrix multiplication, and root determination.

The architecture of the ADSP-1110A, Figure 11, shows several powerful features:

- A 40-bit accumulator (8 extension bits) with overflow detection and overflow flag, especially useful for many-tap FIR filters.
- The option of saturating the output when the overflow flag is asserted; this permits the output to stay at full scale instead of rolling over on a carry. Saturation on overflow avoids the problem of wraparound in twos-complement arithmetic (e.g. when trying to go from +FS to +FS + 1, the output actually goes from +FS to −FS). Among other problems, wraparound can cause full-scale oscillations in an infinite impulse-response (IIR) filter.



FFT "Butterfly" Diagram

- Shift-left-on-output allows the redundant sign bit that may occur in multiplication to be removed and an additional bit of precision gained.
- Independent controls for rounding either the 14th or 15th product bit allow rounding consistent with either a shifted or unshifted output. The combination of shift-left and rounding on the 14th bit produces a properly rounded 15-bit plus sign twos-complement output.
- Broad instruction set allows multiplications to be performed with any combination of signed (twos complement) and unsigned X and Y inputs, and summation in the accumulator using any combination of multiplier and accumulator polarities, i.e., ±XY ± MR.
- A single-bit shift-left-extend register increases the precision that can be obtained in twos-complement operations.
- The ability to transfer the more-significant register to the less-significant register and the extension register to the more significant register is useful for table look-up operations and double-precision operations.

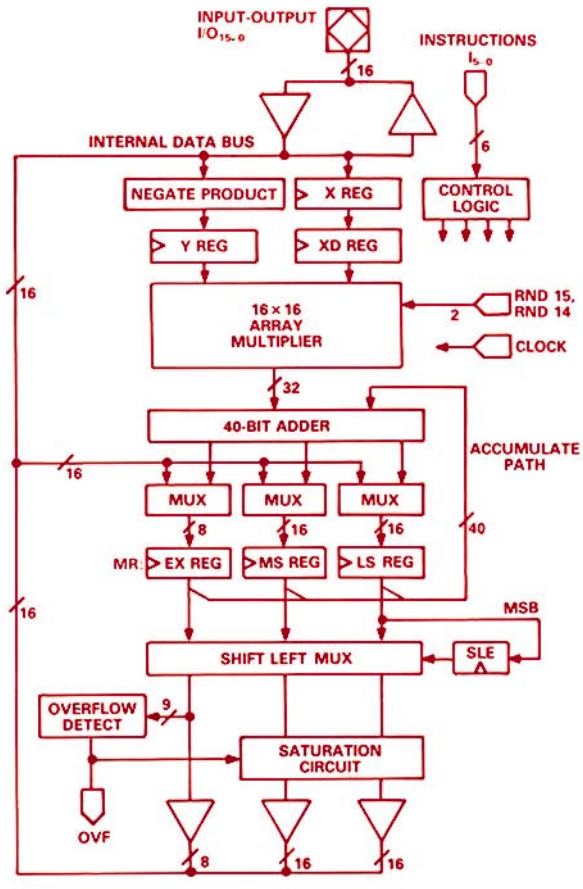


Figure 11. Functional block diagram of single-port multiplier.

Although the ADSP-1110A has only a single port, which must be multiplexed, the apparent throughput penalties (when compared to three ports in most MACs) are minimized by pipelining two input operations with each multiply/accumulate. In this way, the throughput penalty in order to output the final sum of a series of products is limited to only one cycle.

The ADSP-1110A is available in commercial grades (J and K) in plastic or ceramic DIPs and PLCCs for 0°C to +70°C operation. The extended-temperature TD and SD grades (−55°C to +125°C) are available with Analog Devices' commercial high-reliability "PLUS" or MIL-STD-883C processing. Maximum multiply times are 85 ns and 100 ns, with prices starting at $37 and $47 for the J and K grades in 100s, respectively.

*Use the reply card for technical data.

WIDE-BANDWIDTH FAST-SETTLING OPERATIONAL AMPLIFIER

AD9610 Slews at 3.5 V/ns, Settles to 0.1% in 18 ns, Has < 50 dB Distortion @20 MHz

Transimpedance Amplifier Bandwidth Has Little Sensitivity to Closed-Loop Gain

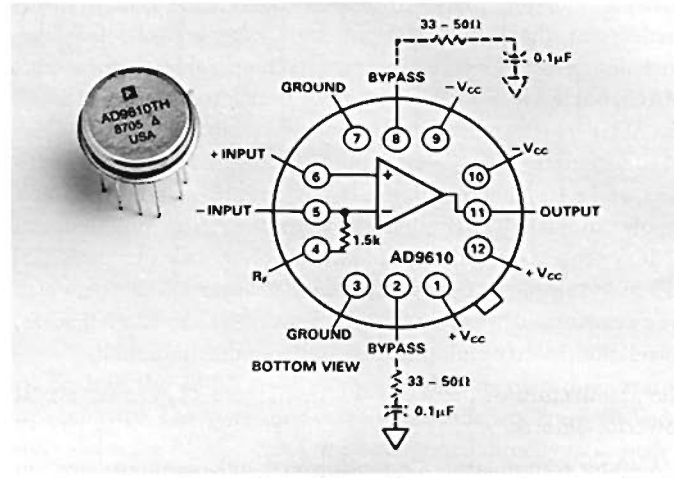
The AD9610* is a wideband dc-coupled operational amplifier housed in a 12-pin TO-8-style hermetic can. It combines exceptional dynamic performance with superior dc specifications at reasonable cost, employing thin-film hybrid technology and innovative design techniques. (Prices start at $49.88 in 100s.)

With its ±50-mA continuous output rating and ability to swing ±9 V with a 200-ohm load (±15-volt supplies), 0.1%-settling time of 29 ns max (−55°C to +125°C, gain of 10, 5-volt output step), slewing rate of 2.4 V/ns min over temperature, and maximum total harmonic distortion below −50 dB at 20 MHz, it is useful for such buffer tasks as driving high-speed a/d converters and unloading high-speed DACs, as well as for pulse-generator outputs and imaging and display drivers. In addition, its ability to maintain bandwidth independently of gain makes it useful in providing wideband gains for photodiode preamps—and radar and intermediate-frequency processors.

Another valuable feature is the character of its recovery from overdrive upsets; this is of special importance in non-ideal circuit environments. After the overdriven condition is relieved, the AD9610 comes out of its saturated shutdown mode without damage or performance degradation.

TRANSIMPEDANCE OP AMP

An unusual aspect of the AD9610 is its use of transimpedance (i.e., current-input-to-voltage-output), instead of voltage-to-voltage gain, in the feedback path. Figure 1 illustrates the basic difference between the two approaches and the results—with "ideal" amplifiers—in the inverting case. The voltage amplifier ideally has high input impedance and gain, A; the error arising from its limited open-loop gain is a direct function of R_F/R_I, which also determines its closed-loop gain (the principle is little different for noninverters, just ground V_{IN} and picture a voltage source in series with the + input; closed-loop gain is $1 + R_F/R_I$). The dc value of A is usually so large that it is not often critical in dc amplification, but the usual 6dB/octave reduction of gain with increased bandwidth results in a tendency towards constant gain-bandwidth; e.g., the −3-dB frequency for gain of +50 is about 1/50 of that for unity gain.



In the second case, Z_{IN} is of the order of ohms (ideally zero), and the output is the product of input current, I, and transimpedance, r_T (of the order of 1 megohm). The ideal closed-loop inverting transfer function is the same (R_F/R_I), but now the gain error depends only on R_F (i.e., if R_F is held fixed and gain is varied by changing R_I only, there is no change in gain error for changes in the ratio, R_F/R_I, even at frequencies for which r_T has decreased). Consequently, the −3-dB frequency for gain of 50 V/V in the actual AD9610, 60 MHz, is better than one-half of the 100 MHz bandwidth for a gain of 1. ■

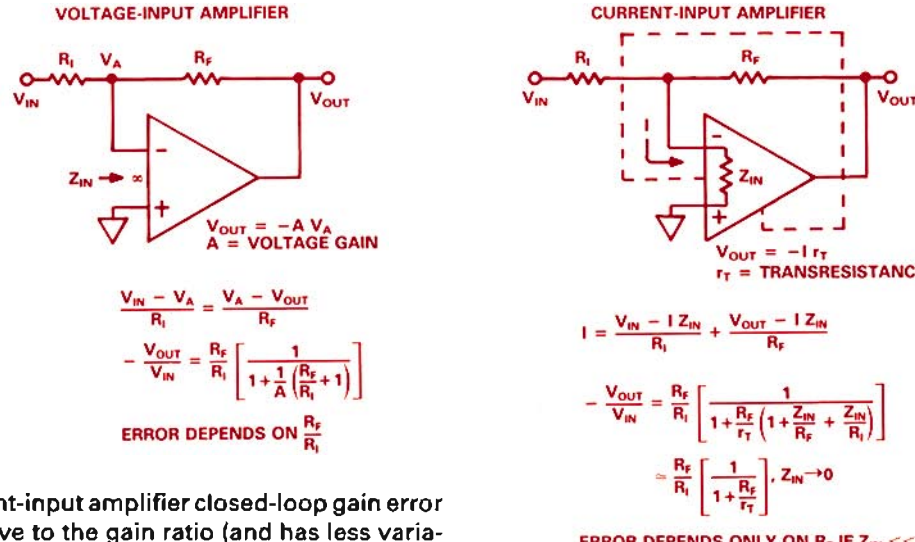


Figure 1. Why current-input amplifier closed-loop gain error tends to be insensitive to the gain ratio (and has less variation of bandwidth with closed-loop gain).

*For complete information on the AD9610—8-page data sheet and 14-page application note—use the reply card.

HIGH-SPEED PIN DRIVER FOR DIGITAL DEVICE TESTING

AD345 Operates at 100 MHz; Has 1 V/ns Slewing Rate, 50-Ohm Output Impedance Drives ECL, TTL, CMOS; Has Low-Leakage Inhibit Mode for I/O Testing

by Bill Gotschewski

The AD345* is a complete high-speed pin driver designed for use in digital functional test equipment and general-purpose instrumentation. It accepts digital, analog, and timing information from system sources and translates them directly to digital output levels to be applied to the input of a device to be tested (DUT).

The output is connected to the DUT via an internal three-state switch (Figure 1); when the switch is opened by a command seen at the differential inputs of the INHibit, the AD345 presents a high impedance to the DUT—an especially useful function when the DUT has an input/output terminal that must be tested without disconnecting the pin driver.

It derives its timing directly from digital sources and its amplitude from analog sources; its output "high" level can be set by an analog voltage at any value from −2 V to +8 V, and its "low" level can be set from −3 V to +6 V; this flexibility makes it compatible with ECL, TTL, and CMOS logic levels and timing. It can drive level changes at up to 100 MHz, with slewing rates better than 1 V/ns; its dynamic output impedance is laser-trimmed for waveform integrity and guaranteed performance with 50-ohm transmission lines. Output impedance is 50 ohms, matching it to coaxial cable used for interconnecting the pin driver and the device's input terminal, in order to minimize error-causing reflections.

By teaming up the economies of surface-mount technology and the accuracies of thick-film laser-trimming, the AD345 attains superb electrical performance while preserving optimum packaging densities in a convenient 10-pin SIP package. Order it as the AD345KY, for 0°C to +70°C operation; it is priced at $115 in 100s.

Who should use the AD345?

Anyone who manufactures or designs equipment for automatic test of semiconductor devices or boards, or for instrumentation and characterization. It can also function as a high-performance, low-cost general-purpose digital driver.

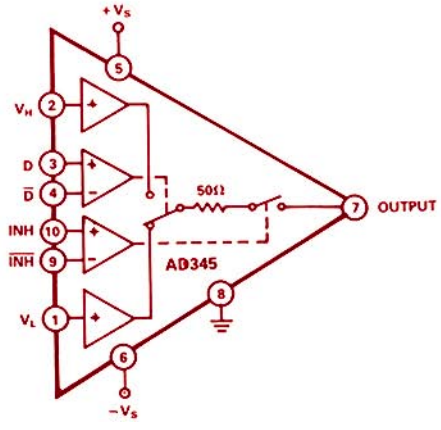
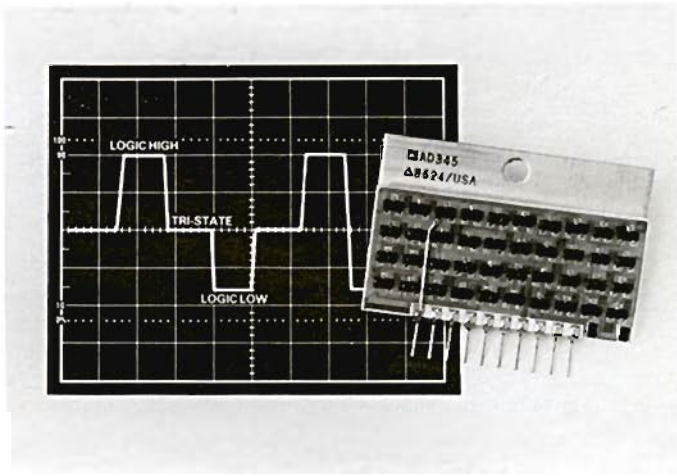


Figure 1. Block diagram of the AD345.

*Use the reply card for technical data.



What is a typical application?

The AD345 has been optimized to function as a pin driver in an ATE test system. The block diagram of Figure 2 (not a wiring diagram) illustrates the components of the electronics behind one of the pins of a high-speed digital functional test system with the ability to test I/O pins on logic devices. The AD345 pin driver, AD96687 (9687-type) high-speed dual comparator, and AD394 quad 12-bit voltage-output DAC would form a major portion of the pin-electronics portion of the test system. Such a system could operate at speeds up to 100 MHz in the data mode or 50 MHz in the I/O mode, yet fit into a neat trim package.

Two of the AD394's four DACs provide precision values for the V_H and V_L logic levels that will be applied to the DUT's input (in the input mode); the other two DACs generate the test levels, V_H' and V_L', that the device's output will be compared against (by the comparators) in the output mode (while the three-state switch is held open by the INHibit signal). The small single-in-line package, with its surface-mount construction, enables the user to place the AD345 in close proximity to the DUT, for optimum signal integrity.

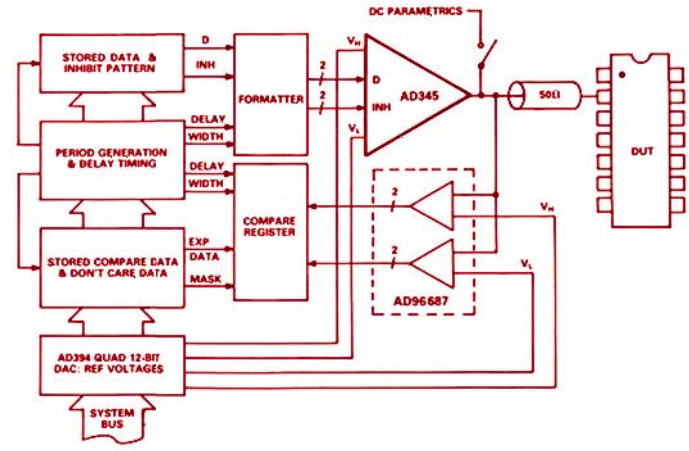


Figure 2. AD345's role in a high-speed digital test system.

MODULAR I/O CARD FOR THE IBM PC

RTI-820: Analog and Digital Inputs & Outputs for the PC, PC/XT, PC/AT
High Channel Capacity, Mixed I/O Types, Can Interface to 5B Signal Conditioners

by Brendon Howe

The RTI-820*, the newest member of the RTI-800 Series of PC Bus boards, is a modular input/output card that plugs into one of the long expansion slots in the IBM PC/XT/AT (or equivalent) personal computer. The board is compatible with a variety of interface panels to allow multiple, mixed I/O to be brought into and out of an IBM PC; it accommodates up to 64 multiplexed analog inputs, 16 multiplexed analog outputs, and 24 1-bit channels of digital I/O. Key features include high channel capacity, 12-bit a/d and d/a resolution, low-cost expansion capability, software drivers for high-level language support, and menu-driven application-software support. Other members of the RTI-800 Series family of boards include the RTI-800 (Analog Input), RTI-815 (Multifunction), RTI-802 (Analog Output), and RTI-817 (Digital I/O).

SUBMULTIPLEXING ARCHITECTURE

Figure 1 shows the architecture of the RTI-820. For flexibility in interfacing, it requires only one channel of analog input and one channel of analog output. Multiple analog I/O channels, which may include isolation amplifiers, signal conditioners, 5B-Series* subsystems, or other high-level analog signals, are expandably accommodated with external interface panels that multiplex a number of input and output channels into the single I/O lines on the RTI-820's analog I/O connector. Decoding lines supplied on the connector control the multiplexing functions of the external interface panels; six input and four output control lines can handle up to 64 signal inputs and 16 outputs.

The multiplexed analog inputs are processed by the RTI-820's sample-and-hold amplifier (SHA) and digitized by a 12-bit ADC at up to 19,000 samples per second. Analog outputs from the 12-bit DAC, and their destinations, are controlled by an on-board slave processor, an Intel 8741, which stores the output values in its internal RAM memory, selects channels, and provides strobe signals for updating multiple SHAs as selected, one at a time. The

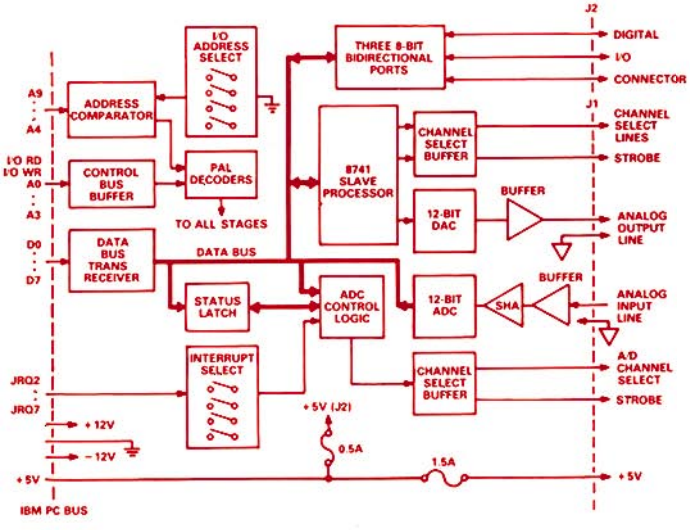
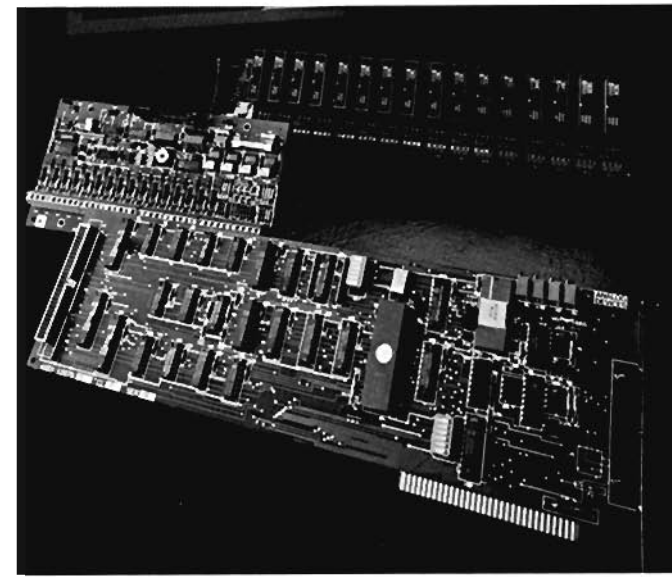


Figure 1. Block diagram of the RTI-820 I/O card.

*Use the reply card for technical data.



8741 can update each of 16 output channels every 2.5 ms (400 Hz per channel), a refresh rate adequate to hold the output voltages stable, depending on the droop-rate specifications of the external SHAs used.

INTERFACE PANELS

Two analog I/O interface panels are available for the RTI-820: the *non-isolated* high-level-voltage panel (STB-HL) has 16 single-ended analog inputs and 4 analog outputs, while the *isolated* signal conditioning panel (5B02) provides 16 analog I/O channels using the 5B Series of signal conditioners. Where its use is appropriate, the STB-HL panel provides an economical signal termination solution by offering low-cost, non-isolated I/O. The 5B Signal Conditioning Modules, on the other hand, offer high-performance at low cost for multi-channel industrial signal conditioning. The panels are compared below.

Model	Channel Capacity	Input Types	Output Types	Isolation	Power Required
5B02	16 Analog I/O	Thermocouple, RTD Current, Voltage	Current (Voltage)	+2,000V	Depends on Modules Used
STB-HL	16 AIN (SE), 4 AOT	High-Level Voltage	Voltage	No	+5V@350 mA

A 3 ft. ribbon cable (CAB-01) is used to connect any of the interface panels to the RTI-820. Each cable has a second connector to connect additional CAB-01's in daisy-chain fashion. Up to 4 panels, in any combination, may be connected in this manner to provide multiple, mixed analog inputs and outputs.

The digital I/O channels of the RTI-820 also have two panel options: a nonisolated screw-termination panel (AC1585-1) provides direct connection to TTL-level inputs and outputs, while the DB-24 solid-state relay subsystem provides the interface to high-level digital sensing and switching with ±4,000-volt isolation. Digital I/O channels are brought to the RTI-820 through a separate 50-pin digital I/O connector.

PROCESS MONITORING & OPERATOR INTERFACE SOFTWARE FOR μMACs

CAMM Applications Software Links μMAC Family as Front End, Provides IBM PC-Based System with Powerful Real-Time User Features

by Doug Green

The Analog Devices μMAC-5000* and μMAC-6000* provide real-world input/output and signal processing for industrial processes. Most applications in the plant or factory also require an operator interface to display current conditions, monitor key points for alarms, log desired data, and analyze and display trend information. That interface is provided physically by a host computer and its display screens; computer programs determine at the machine level what the computer must do to meet these needs, and at the operator level what information must be acquired and how it is to be communicated and handled. The CAMM software package, now available from Analog Devices, is designed to run on the IBM PC family and link powerful process-monitoring software and operator interface screens to μMAC programmable measurement & control subsystems. It consists of a set of disks and manuals.

CAMM (Computer Aided Manufacturing Management) was developed by CENTEC Corp. to provide an integrated set of software modules that support management, and the manufacturing and engineering staff, in operating, analyzing, and managing the manufacturing facility. Each module provides a unique set of functions; the user purchases only those modules actually needed for the desired functions. CAMM runs on the IBM PC under the standard MS-DOS operating system; it communicates with the μMACs via MCComm, a communications protocol that is available from Analog Devices for the μMAC and MACSYM families of products. For reliability, actual process control is implemented on the local level, with μMAC resident programs written by the user. The user configures CAMM to periodically access data from the various sensors to be monitored. CAMM's flexible data-logging capability allows different logging strategies to be automatically implemented when needed—for example, the sampling rate for a given channel may be increased when the channel input approaches a critical condition.

The user configures and operates CAMM with menus; CAMM is entirely menu driven. It is a sophisticated program written primarily in Pascal with over 150,000 lines of code—all of which is transparent to the user. High-quality graphics, in color, can be created to dynamically model the ongoing processes in real time. These graphic displays can be created from an existing library of shapes, or new shapes can be created if needed. With the μMAC and PC hardware, CAMM provides these four overall functions:

Collects status data from the process CAMM continuously and repeatedly gathers the latest values of selected points, such as sensor input values, control output levels, and setpoint values. These are all called "sensors" within CAMM; they can be in unscaled units or converted, scaled engineering units.

Makes a record of each sensor value collected from the process and stores the records in a permanent log file These log files can be displayed as tabular or graphical reports by CAMM (Figure 1); they can also be used by other software programs, such as LOTUS 1-2-3, for special reporting and analysis.

*Use the reply card for technical data.

Figure 1. CAMM screen shows graphic panel with acquired data and system status in tabular form.

Provides a complete operator interface to the process. CAMM displays the collected data to the user in a variety of formats (Figure 2). The user can supervise the process by directly sending new instructions, such as setpoint value changes. All critical process parameters are password-protected.

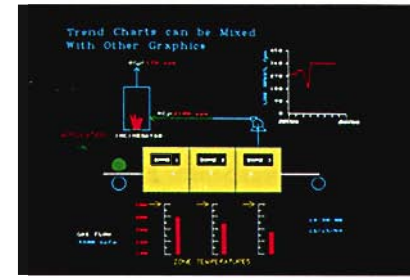


Figure 2. Operator screen graphics showing mixture of trend charts and other graphics.

Supports in-depth data analysis. CAMM provides a full set of tools and reports that process engineers and managers can use to analyze and improve the processes.

As many as 1,000 sensors can be handled by equipment using CAMM, with up to 250 logged at one time. A maximum of 32,756 sensor readings may be stored in a data logging file. Since the graphics screens are stored as DOS files, there is no practical limit on the number of screens that can be used.

Internal Architecture

CAMM organizes the computer into a workspace having a number of functions that work together and pass information among each other as required (Figure 3). A set of modules make use of interactions within this workspace to perform user functions; the CAMM user has to purchase only the modules required for the application (although certain modules—which essentially organize the workspace—are a part of every installation). The modules available include a system key module, an online logging module, an offline setup module, analytical modules, and graphics and display modules:

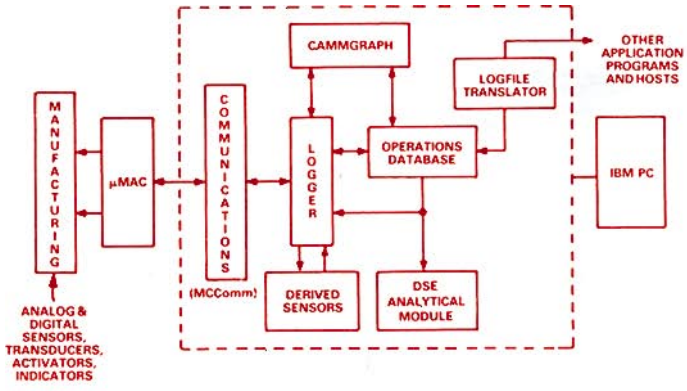


Figure 3. Block diagram shows how the various CAMM functions are integrated with one another.

The System Key Module (CAMM-01) is a part of every CAMM installation. It includes the system key disk with installation program, security hardware key, and documentation binder.

The Online Logging Module (CAMM-02) communicates with the μMAC controllers using the MCComm protocol to obtain data and log the data into the CAMM operations database. Once the logging function is turned on, it will continue to operate in the background even if other software modules are being used. The logging module receives its data sampling and logging instructions from the:

Off-line Setup Module (CAMM-03). This module, which sets up the logging model, is generated by the manufacturing engineer by simply filling in a table in response to questions. This module is required for configuring and modifying the processes, but not for installations which only need to have monitoring and analysis capability.

The *Analytical Module* provides one of two ways of utilizing the data logged by CAMM (CAMMGraph is the other); it comes in two versions. The DSE (Direct Sensor Entry) Analytical Module-EGA, CAMM-04, prepares and displays spreadsheet reports using real-time data and can chart data on-line. A sensor "reading," which can be actual acquired data or derived by calculations from an actual data point or combination of points, is specified in a cell in the same manner as an equation in an ordinary spreadsheet. Once the sensor date and time are specified, the analytical module provides the corresponding value, which can then be used in subsequent calculations.

To allow the data to be used by other software programs, the module provides the DIF format for the data, which means that it can be loaded into other compatible software packages. The IBM PC must have the EGA graphics adapter installed to use this module. The other version is the DSE Analytical Module-L, CAMM-05, is similar to CAMM-04 but does not support the high-resolution EGA adapter. Instead, it uses the CGA adapter for medium-resolution charts and graphs.

The CAMMgraph Setup Module-EGA, CAMM-06, is used to create or modify display templates. It allows the user to build templates, which form graphic "windows" through which the operators view the real-time operation of the process. Templates can represent the process, changing in form to illustrate changes in log data. They can depict simple line diagrams or complex schematics and floor layouts. The user can copy templates from other configurations or from an existing shape library. Graphics are stored in a high-resolution 20,000 × 25,000-point matrix and then reduced to match the display being used. This module is needed for configuring and modifying process graphics, but not for installations that just need monitoring and analysis. Like CAMM-04, it requires the EGA adapter in the IBM PC.

The CAMMGraph Display Module (CAMM-07) allows graphic display of data in real time or in playback modes. It can display all the color graphic process templates. It also animates the templates that were previously created, to attach any sensor states (such as high temperature) to any shape, set of text, or fill color (too hot becomes red text and filled in area, for example). Any shape can be made to move within the process template. Alarm messages, diagnostic messages, sensor values, time, date, or any desired text can be used with any process template.

CAMMGraph also allows for graphic display in a playback mode, which reviews past performance at rates from one-fifth to 125 times the actual data-acquisition rate. It is similar to fast forward and slow motion in a video tape recorder, except that the acquired sensor database is used as the source of information.

In order to execute, CAMM requires an IBM PC-XT, IBM PC-AT, IBM 5531, IBM 7531, IBM 7532, IBM 7552 or Analog Devices MACSYM 120 with a hard disk of at least 5 Mbytes, 640 kB RAM, a serial RS-232 port, the math coprocessor for the CPU (i8087 or i80287 where appropriate), and PC DOS (or MS DOS) operating system versions 2.1, 3.0, 3.1, or 3.2. An IBM EGA Adapter, with 256K RAM installed, and Enhanced Color Monitor may also be required.

Most CAMM users will choose one of two CAMM configurations. The full-feature configurations include on-line logging, analysis, and process-modelling graphics. It consists of CAMM-01, -02, -03, -04, -06, and -07. A less-expensive version of CAMM, with CAMM-01, -02, -03, and -05, includes on-line logging and analysis, but does not have the process-modelling graphics capability. The modularity and flexibility of CAMM can be also used to develop configurations with different capabilities, such as for logging only, monitoring but not setup (to restrict the operator's ability to change the system setup), or to allow an additional PC to perform analysis offline using previously generated log files (Figure 4).

CAMM MODULES NEEDED FOR CAPABILITIES AT LEFT

	-01	-02	-03	-04	-05	-06	-07
FULL CAPABILITIES & PROCESS GRAPHICS	✓	✓	✓	✓		✓	✓
WITHOUT PROCESS GRAPHICS	✓	✓	✓		✓		
LOGGING ONLY	✓	✓	✓				
RESTRICTED (NO SETUP) SYSTEM	✓	✓		✓			✓
RESTRICTED WITHOUT GRAPHICS	✓	✓		(✓ OR ✓)			
ADDITIONAL PC	✓			(✓ OR ✓)			

Figure 4. CAMM modules can be combined in different ways depending on the application.

PRECISION SIGNAL CONDITIONER FOR BRIDGE TRANSDUCERS

Chopper-Stabilized 1B32 Has Low Tempcos: ±0.07 μV/°C Offset, ±2 ppm/°C Gain
Includes Adjustable Excitation and Built-In 3-Pole 4-Hz Filter

by Amer Iqbal

Model 1B32* is a complete, chopper stabilized signal conditioner that interfaces directly with load cells and pressure transducers and produces a filtered high-level output. A cost-competitive solution for in-house signal conditioning system designs, it is ideal for OEM designers who require 14- to 16-bit accuracy in weighing-scale applications.

The 1B32 comprises a precision chopper amplifier, a low-pass filter, and an adjustable excitation source in a compact 28-pin plastic double DIP (Figure 1). Its price (100s) is $52.

Chopper Amplifier The chopper-based amplifier features extremely low input offset tempco (±0.07 μV/°C at G = 1,000), low nonlinearity (±0.005% max), low input noise (1 μV p-p, 0.1 Hz to 10 Hz), and high common-mode rejection (140 dB minimum at 60Hz, G = 1,000). An offset-adjustment terminal permits the input to be offset by as much as ±10 volts, for nulling dead loads or adjusting for tare weight. A thin-film network provides gains of 333.3 and 500, which are required to get a 10-V output from load cells with 30-mV and 20-mV spans. The gain tempco for these fixed gains is a stable ±2 ppm/°C. Alternatively, the gain can be set to any value between 100 and 5,000 with two external resistors.

Filter The three-pole low-pass filter has a corner (cutoff) frequency of 4 Hz, which is typical in precision weighing applications. Normal-mode rejection is 60 dB per decade above the cutoff frequency.

Excitation DC bridge excitation is provided by an adjustable-output regulated supply with an internal 6.8-volt reference, and a factory-set output of +10 volts. Any output value from +4 V to +15 V can be set by using an external resistor to adjust the gain of the regulator amplifier. The 1B32 is rated to furnish up to 100 mA of output current at +25°C.

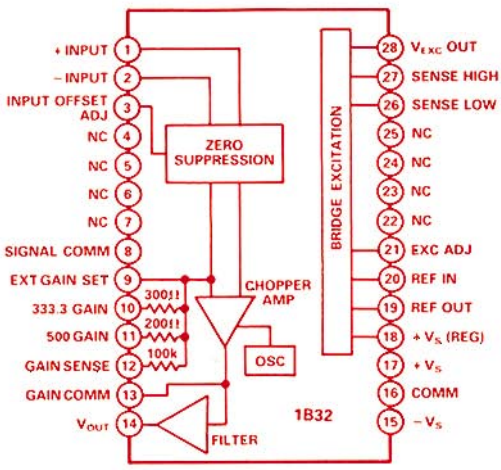
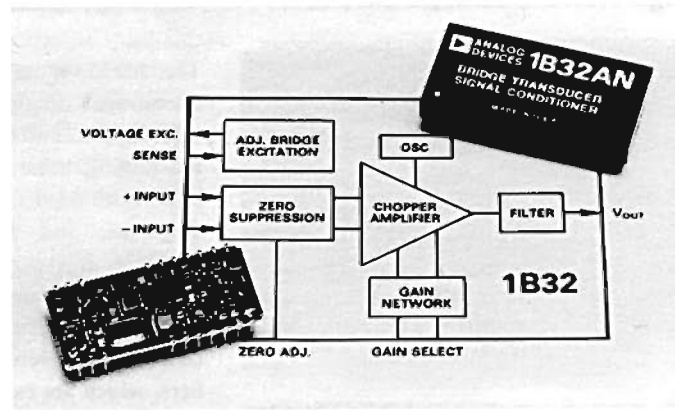


Figure 1. The 1B32 performs precision amplification, bridge excitation and filtering.



Two features of the 1B32 that make it especially suitable for precision load-cell interfacing are remote sensing and laser-trimmability for arbitrary values of gain. For applications where lead resistance causes significant voltage drops, the high-impedance SENSE inputs use feedback to enforce the precise value of the excitation at the destination. For applications where the transducer output or the a/d-converter input level is non-standard, and a large number of 1B32 units must be connected for special values of gain, costs can be reduced by purchasing the 1B32 with the gain laser-trimmed to user specifications. Get in touch with the factory for further information.

Typical applications for the 1B32 are in weighing systems and precision scales, where 1-in-10,000-count accuracy is required by Federal standards; in avionic system testing, where the small size is of great advantage in multi-channel designs; and for signal-conditioner designs employing plug-in cards for personal-computer data-acquisition systems. Figure 2 outlines a two-package solution for precision amplification and 18-bit a/d conversion using the 1B32 and the AD1170*, which nulls fixed offsets digitally and does periodic full-scale calibrations.

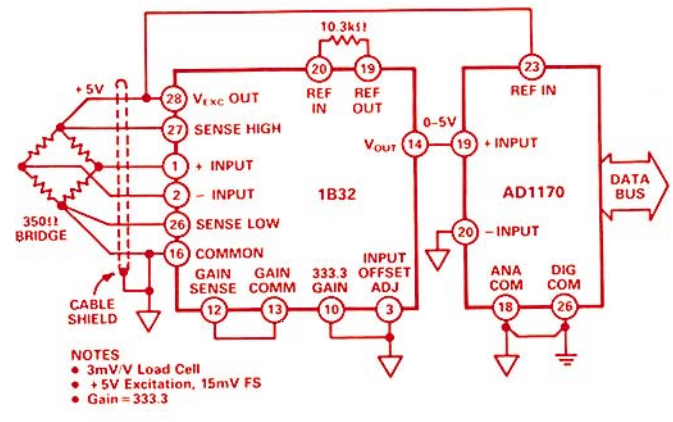
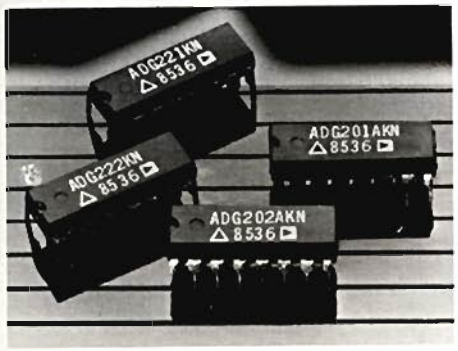


Figure 2. Auto-calibrating data acquisition uses the 1B32 as a front end for the AD1170 a/d converter.

*Use the reply card for technical data.

CMOS SWITCHES

Four Quad SPST Devices: High Performance, Low Cost



The ADG201A/202A* and ADG221/222* family of quad single-pole, single-throw CMOS switches are characterized by high performance and low price. The switches of the ADG201A/202A are operated directly, while the ADG221/ADG222 are operated via internal microprocessor-compatible latches. The ADG201A and ADG221 are ON for logic 0, OFF for logic 1; the ADG202A and ADG222 are ON for 1, OFF for 0.

All devices have a breakdown range of 44 volts, an analog signal range of ±15 V, and typical leakage current of 500 pA. They are available in four grades that are guaranteed over three temperature ranges: the KN grade, 0°C to +70°C; BQ grade, −25°C to +85°C; TQ and MIL-STD-883C military grades, −55°C to +125°C. Packaging options include plastic, cerdip, LCC, and PLCC. Prices (100s) start at $2.56 for the latched versions and $3.15/$2.95 for the ADG201A/202A.

ADG201A performance parameters (25°C) include: 90-ohm max R_{ON}, 1 nA max leakage current, 300 ns max t_{ON}, 250 ns max t_{OFF}, and 33 mW max power dissipation. Switches are break-before-make. There are existing second sources bearing similar generic type numbers for all of the devices except the ADG222, which stands alone as a "reverse-logic 221" latched quad switch.

The parameters of the new devices are comparable to or better than those of most existing second sources, especially max t_{ON} and t_{OFF}, and min t_W and t_S (100 ns)—which are important specifications in microprocessor applications.

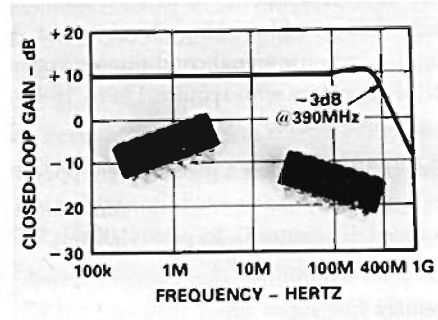
*Use the reply card for technical data.

MONOLITHIC OP AMP SETTLES TO 1% IN 12 ns

AD5539 Has 600-V/μs Slew Rate, 82-MHz Full-Power Response 220-MHz Unity Gain-Bandwidth, 1.4-GHz GBW Product

The AD5539* is an ultra-high-frequency operational amplifier designed for use in video circuits and r-f amplifiers. With its 12-ns settling time to 1%, typical gain-bandwidth product of 1.4 Ghz, slew rate of 600 V/μs, and full-power response of 82 MHz, it represents a substantial improvement over comparable pin-compatible 5539 op amps; it is a significantly better choice than currently available GaAs amplifiers, which are expensive, noisy, and have poor dc performance.

In addition to its fast dynamic specs, the AD5539 has max dc error specs that are tested and guaranteed over temperature: 6 mV and 5 mV input offset voltage (J and S grades), 5 μA and 3 μA input offset current, and 40 μA and 25 μA bias current. Minimum open-loop gain is 47 dB; minimum CMR is 70 dB, and input voltage noise spectral density at frequencies above



100 Hz is 4 nV/√Hz.

Typical uses include amplifying fast pulses, video signal processing, and rf oscillators. Video displays, radar, communications, and guidance control systems are just a few of the intended application areas. It operates from ±8-V supplies, dissipates 500 mW, and is available in 14-pin plastic DIP and cerdip for 0°C-70°C (J), and cerdip for −55°C to +125°C (S). Prices start at $1.65 (100s).

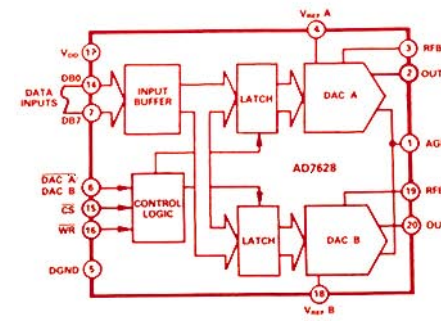
CMOS DUAL 8-BIT MULTIPLYING DAC

AD7628 Has Two Latched DACs, TTL/CMOS-Compatible +12-V to +15-V Power Supplies; 20-pin DIP, LCC, PLCC

The AD7628* is a dual 8-bit multiplying digital-to-analog converter that operates on +12- or +15-volt supplies and is CMOS/TTL-compatible. It is useful where there is a need for multiple DACs, such as in personal computer add-on boards, disk drives, X-Y graphics, or programmable filters.

The AD7628 is bus-compatible with most 8-bit microprocessors, including the 6502, 6809, 8085, and Z80; its on-chip DACs are individually buffered for easy μP interface. Data is transferred into either of the two DAC latches via a common 8-bit TTL/CMOS-compatible input port. Control input $\overline{\text{DAC A}}$/DAC B determines which DAC is to be loaded.

Matched to 1%, the DACs are capable of operation in either current (4-quadrant multiplying) or voltage (single-polarity supply)



modes. Power dissipation is a mere 20 mW.

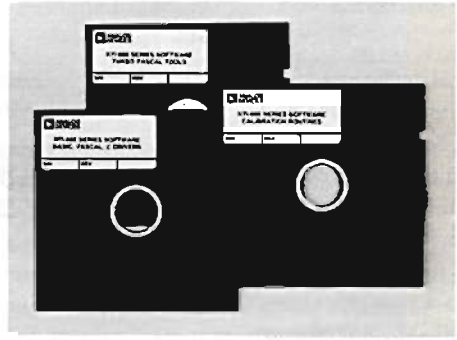
Max error over temperature is ±½ LSB (relative accuracy), ±3 LSB (gain), and ±1 LSB (differential linearity). The AD7628 is available in three temperature grades (K/B/T) and four packages (0.3" 20-pin DIP—plastic or cerdip—and LCC or PLCC). Prices start at $5.60 in 100s.

TEST DEVELOPMENT FOR BENCHTOP TESTERS

LTS-2020TDS Generates and Tests Component-Test Programs Programmable in Basic and Fill-in-the-Blanks 'CREATE'

The LTS-2020TDS* is a new test-development station designed to generate and edit test programs for the Analog Devices LTS-2020* benchtop component-test system. The TDS, a subsystem of the tester, is designed for use in test environments and features the same standards of reliability as the LTS-2020 tester. The TDS shifts critical software development from the production floor to a desk top, minimizing downtime and providing a faster, less-expensive method for developing test programs.

The LTS-2020 has become an industry standard in benchtop component testing; it is the first benchtop tester to combine ac digital testing with linear, passive, data conversion, and discrete device test capability. The TDS provides complete compatibility with all LTS-2020 software and is programmable in



Basic and fill-in-the-blanks CREATE. Its 512 K bytes of memory can support LTS networking.

The complete test station includes a small portable case, two 5.25" double-density, double-sided half-height disk drives, a 14" CRT, and full computer keyboard with 32 user-programmable function switches. Price of the TDS is $6,990.

NEW SOFTWARE RELEASE FOR RTI-800 SERIES

AC1527-A for IBM PC/XT/AT Operates Under MS-DOS & PC-DOS More Efficient, Easier to Use; Improved Drivers—Less RAM

The AC1527-A is a utility software package for the Analog Devices RTI-800 Series of personal-computer-compatible boards for IBM PC/XT/AT. Operating under MS-DOS or PC-DOS, the software provides the user with subroutine calls to access the input/output functions of all existing RTI-800 series boards. I/O functions that are supported include analog I/O, digital I/O, frequency input, event counting, and pulse output.

This improved software package, a new release of AC1527, consists of high-level-language libraries, hardware libraries, and a sample program. It is a software tool to help RTI-800-Series users develop custom application programs. The I/O routines (AIN, AOT, etc.) can be called directly from a high-level language, eliminating the need for a user to write software routines in assembly language.

The software package includes such features as a menu-driven configuration program,

error-handling routines, an initialization routine, and menu-driven calibration software. Eight languages are supported, including IBM Compiled Basic and Interpreted Basic, Microsoft's Compiled Basic, C, Pascal, FORTRAN, Macro Assembler, and Borland International's Turbo Pascal. Price is $295.

*Use the reply card for technical data.

ASYST FOR RTI-800

Application Software for Lab, Scientific Data Acquisition

The RTI-800 Series of IBM PC-compatible plug-in data-acquisition boards are now supported by ASYST™ Scientific Software (from MacMillan Software Company), available through Analog Devices in two versions. ASYST is a programmable software package featuring a set of engineering and scientific tools for low-point-count data-acquisition applications in labs, using I/O cards in an IBM PC.

Typical users include scientists and engineers having some familiarity with programming languages and needing large amounts of software flexibility and power for handling data-acquisition and analysis tasks in R&D labs and pilot plants.

It's easy to use. The user installs RTI-800/815 cards in an IBM PC/XT/AT; boots up ASYST Module 1 (basic system software, including graphics and statistical functions), Module 2 (analysis algorithms, including FFT), Module 3 (RTI-800 Series drivers), and—optionally—Module 4 (IEEE-488 communications); connects to instruments; and programs in an easy to learn, interactive, unstructured language.

The result is an integrating instrument interface in a single package, with powerful data reduction, analysis, and graphics capability. The building-block approach and the flexibility of its programming language mean time savings in developing an application.

ADI's ASYST options support up to 32 analog inputs with maximum I/O rates of 26 kHz in normal mode, using a single channel, and 70 kHz in DMA mode, using the PC/AT. The ASYST package is priced at $2,060; RTI-800/815 boards start at $850/$1,095 (1s).

Worth Reading

NEW FREE PUBLICATIONS FROM ANALOG DEVICES

DSP Applications Handbook

184-page Applications Handbook for the ADSP-2100 single-chip DSP microprocessor—a compilation of routines for a variety of common digital signal-processing applications. Includes chapters on fixed- and floating-point arithmetic, fixed-coefficient digital filters, FFTs, adaptive filters, image processing, and linear predictive speech coding. Request it from your nearby ADI sales office.

Catalogs and Brochures

*1987 Military Products Databook** 700 pages of device specifications for both monolithic and hybrid products manufactured and tested in compliance with the latest revision of MIL-STD-883. Its 145 product types include op amps, instrumentation amplifiers, analog signal-processing components, voltage references, temperature-measurement components, DACs, ADCs, VFCs, DSP components, S/H amplifiers, data-acquisition subsystems, and CMOS switches & multiplexers—in a variety of packages, including CLCC. Of these products, 21 have JAN (MIL-M-38510) part numbers, another 6 are available against standard military drawings.

*PC Bus-Compatible Products 1987** More than 114 pages of data on RTI-800 Series hardware & software products, signal conditioning modules & subsystems, and technical notes.

Word-Slice User's Manual 225 pages of functional descriptions, examples, and detailed reference of the instruction sets for present & future designers of microcoded systems using the ADSP-1401 Program Sequencer and ADSP-1410 Address Generator. Request this manual from your nearby ADI sales office.

*Surface-Mount Integrated Circuits** 28-page brochure reviews 46 advanced data-acquisition products available in plastic surface-mount packages (PLCC and SOIC). Block diagrams, specifications, and pinout & packaging information are provided.

*High-Speed Data Conversion** is a 20-page Selection Guide to fast ADCs, DACs, track/holds and amplifiers.

"Straight Facts About Purchasing Op Amps"* is a 16-page guide designed to aid purchasers of op amps in understanding ordering procedures, lead times, part numbering and package variations, op amp types and specifications, manufacturing processes, and MIL-STD 883 programs.

Industrial Automation Products 1987 (234 pages) Technical notes and catalog on products for real-world I/O, with ordering guide to board interface products. Available from systems sales force.

Recent Issues of Newsletters from Analog Devices

Analog DSPatch—The Digital Signal Processing Newsletter* Volume 1, No. 3 (12 pp): The ADSP-1101 Integer Arithmetic Unit; third-party products using or supporting ADSP parts; Q & A; user notes and other news (ADSP-2100 safely launched from 155-mm howitzer—12,265g!); listing of available DSP literature.

Analog Briefings—The Newsletter for Military/Avionics Industry, II-3, III-1, III-2 (6 pp. each): Upcoming-product briefings; new QPL DACs (AD561, AD565); updates to *Military Products Databook*; qualification status of ADI products; Analog Devices Semiconductor Recertification; Standard Military Drawings; 883 version of ADSP-2100; Section B (MIL-STD-1772) hybrid qualification; European military standards.

*Use the reply card to request a copy.

MORE AUTHORS (Continued from page 2)

Alan Hansford (page 8) is a Marketing Engineer with the IC product group at ADI's Computer Labs Division, in Greensboro, NC. He currently holds a BSEE from the University of Virginia. Before joining Analog Devices, he provided technical applications support for the High-Speed Linear Group at Harris Semiconductor. Alan enjoys building furniture and studying architectural styles.

Brendon Howe (page 14) is a Marketing Engineer in the Board Interface Group at ADI's Industrial Automation Division. He has been with the Company for three years, previously working as an Applications Engineer for the Measurement and Control Group. He has a BSEE from Boston University and worked as a Design Engineer at Raytheon's Computer Laboratories before joining Analog Devices.

Amer Iqbal (page 27) has been promoted to Senior Marketing Engineer at ADI's Interface Products Division. A biographical sketch and his photo appear in Volume 20, Number 2 (page 2).

Richard Parker (page 23) is the Deputy Marketing Manager for ADI's Memory Devices Division in East Molesey, England. He joined the Company in 1980 and has held various positions in Marketing, including two years based in Norwood, Massachusetts. Richard holds a Physics degree from Oxford University.

Bill Thompson (page 12) is a Marketing Engineer in the Converter Operating Group at Analog Devices Semiconductor. He earned a BSEE from Union College, in Schenectady, NY. Before joining Marketing, he held the position of Group Leader in the ADS Converter Operating Group's Product Engineering group.

Tom Tice (page 9) is an IC Project Engineer on high-speed a/d converter design at ADI's Computer Labs Division. Before joining Analog Devices, he was engaged in instrumention design at R. J. Reynolds Industries. He received a BSEE from North Carolina State University in 1983. In his spare time, he designs and builds stereo hi-fi equipment and plays golf, racqetball, and volleyball.

Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

PRODUCT NOTES . . . The AD7590DI Series of dielectrically isolated CMOS analog switches with on-chip latches for uP interfacing has been improved: dynamic specs are faster (switch-on, switch-off, and transition time); for hermetic packaging, cerdip replaces side-brazed ceramic; and grades that operate at MIL temperatures have been introduced. Ask for the new data sheet . . . Reliability data on the ADG201A switch family is available: high-temperature life test and biased humidity test (plastic parts). Consult your local ADI sales engineer . . . Demonstration boxes for the AD651 monolithic synchronous V/f converter (see the last issue) are in the hands of the ADI Sales force - 16-bit conversion off a +15-volt supply for a 0-to-10-volt input range. If you think the AD651 might be useful to you, call your local Analog Devices sales office . . . 2Kx8, 16Kx4, and 8Kx8 memory ICs suitable for the ADSP-2100 are available from a number of manufacturers, such as Cypress, IDT, and Lattice Semiconductor . . . KIT150 is a combination of hardware and software that makes it possible, using popular 3rd-party PC-DOS software, to analyze or present data previously gathered by MACBASIC programs. Call your ADI systems sales engineer . . . The AD246JN Clock Driver in a DIP package is now available for isolator systems (up to 32 channels) using DIP-packaged AD204 isolators. NOTE: Please disregard outline dimensions and pinout information for AD246JN on AD204 family data sheets printed prior to 12/86; a correct drawing is available from your nearby sales office . . . When groups of 3B17 LVDT signal conditioners are used on the same 3B backplane, their oscillators can be synchronized. For information, call 1-800-245-3900 and request the Product Note: "Multiple LVDT Installations" . . . The AC1222 mounting card is available with all components necessary for evaluating the 1B31 Strain-Gage Signal Conditioner (see the last issue); for information, consult the ADI sales force.

IN THE LAST ISSUE

Volume 20, Number 2, 1986 – 28 Pages

Editor's Notes, Authors

Fast, Flexible CMOS Single-Chip µP for Digital Signal Processing (ADSP-2100)

Monolithic 16-Bit DAC is 16-Bit Monotonic – All Grades and Temp Ranges (ADS69)

The 5B Series: Compact Low-Cost Plug-In Signal Conditioning Modules

µMAC-6000: An Expandable Modular I/O Processor for Industrial Automation

Precision Wideband 3-Port Hybrid Isolation Amplifier (AD210)

Monolithic Synchronous V/F Converter: 0.005% Max Nonlinearity (AD651)

High-Linearity 16-Bit DAC Is Digitally Trimmable (AD1147/AD1148)

Small, Fast, Low-Cost, High-Resolution Integrating A/D Converter

Low-Cost Hybrid Strain-Gage Signal Conditioner (1B31)

The Easy Way to Interface an LVDT to Digital (2S56 converter family)

New-Product Briefs:

- Dual 12-Bit DACs in 0.3" DIPs for 8/16-Bit Data Buses (AD7537/AD7547)
- Highest-Performing Low-Cost BiFET Op Amps (AD548/AD648/AD711/AD712)
- AD202/AD204 Isolator Family Enhanced (K versions and low-profile DIPs)
- High-Resolution Programmable-Gain DAS (AD367)
- Data Acquisition and Processing for PCs – RTI-800s & Commercial Software
- LCCs, PLCCs, and SOICs: ICs Available in Surface-Mount Packages
- Unity-Gain Buffer Amplifier with 200-MHz Bandwidth (HOS-200)
- Complete 12-Bit, 5-MHz A/D Converter (with T/H) on Eurocard
- 12-Bit Multiplying DAC with 110-ns Settling Time
- Fast, User-Reprogrammable OCR Reader, SPEED READER™
- Analog Output Module for µMAC-5000 (QMXAO)
- µMAC-5000 Runs C – Software Tools for New Programming Option

New Literature and More Authors

Potpourri

Advertisement

DATA SHEETS AND SPECIFICATIONS . . . AD7115 specification change: Write pulsewidth, t_{WR} at 25°C, 1 microsecond; t_{WR} T_{min} to T_{max}, 1.24 microseconds . . . AD7576: Conversion time with internal clock is now 30 µs max for all grades; device-to-device clock-frequency variation (page 7 of data sheet) is 50% . . . 1986 Update and Selection Guide (p. 3-233): In data for AD7547, please correct pin connections on block diagram - WR is pin 19 and CSB is pin 20. Loose data sheet is OK . . . New AD574A data sheet (5/87) is available with expanded applications section and improved performance specifications . . . HAS-1204 data sheet (11/85): In Figure 4, Unipolar and Bipolar "APPLY" test inputs should be -FS + 1 1/2 LSB and -FS/2 + 1 1/2 LSB, respectively . . . CAV-1205 data sheet (5/86): Under "Ordering Information," the analog input range must be specified by the user - order CAV-1205-1 for ±1.024-V input or CAV-1205-2 for ±2.048-V input . . . AD9703 data sheet (10/86): Thermal resistance and MTBF are incorrect; correct figures for junction-to-air and junction-to-case are 48 and 10°C/W, and MTBF should be 1.2×10^5. The temperature condition in footnote 11 is +70°C Case . . . ADSP-1008A specs (3/87)have improved. MAC times for J/K/S/T are now: 60/50/75/60. Data setup times are now 15 ns (vs. 20 ns); power consumption has increased to 200 mW (but still less than 1/10 the dissipation of the part they replace) . . . DAS1150: Bias current spec is now 80 nA typical.

MILITARY AND PACKAGING . . . For information about the transition from side-brazed ceramic (D) packaging to cerdip (Q) packaging, consult the Components sales force . . . Additions to QPL: AD561 10-bit current-output DAC, JM38510/13301BEA, and AD565 12-bit DAC, JM38510/12103BJC, are now available for customers who must use JAN parts . . . The AD574 12-bit a/d converter can now be ordered (both AUD and ATD grades) on a Standard Military Drawing (SMD): 5962-85127 . . . The AD2700 and AD2702 precision references, SD and UD grades, are now specified by DESC Military Drawing 85030 (rev A) . . . The AD651 synchronous VFC is now available in an 883 version. Consult the ADI sales force . . . The AD637 rms-to-dc converter is now packaged in cerdip - same specs and pinout as the side-brazed version.

U.S. PATENTS . . . 4,622,512 to Adrian P. Brokaw, for "Band-Gap Reference Circuit for use with CMOS IC Chips . . . 4,639,683 to Lewis W. Counts and JoAnn P. Close, for "Very low input-current JFET amplifier.

THE BEEP IS: WHERE'S THE NOISE? . . . We received a query from erstwhile colleague, Bob Pease, of National Semiconductor, regarding a scope plot in Analog Dialogue 20-1 (Figure 2 on page 16). He thought there was something fishy about the 0.01%-settling-time plot comparing 4 examples for a range of gains from 1 to 500; the noise seemed to remain just about the same, which somehow defied logic, since it implied an unbelievably quiet amplifier - which was not in accord with our published specs for the device. The answer was: through the miracle of modern oscilloscopy, our new-fangled digital scope had itself filtered out the noise automatically - permitting a clean, coherent, and credible - if improbable - comparative plot of settling at high gain. That this wondrous new technology has the potential for creating misleading inferences, despite the best of intentions, gives us all something to think about!

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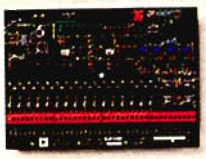

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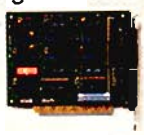

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3	5B02	Analog Signal Conditioning I/O Subsystem
24	5B37	Isolated Thermocouple Input Module
2	DB-24	Digital I/O Subsystem
5	IA120Q	4-Channel Isolated AC Input Module
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